GC4114

QUAD TRANSMIT CHIP

DATASHEET

May 22, 2000

Rev 1.0

This datasheet contains information which may be changed at any time without notice.

REVISION HISTORY

Revision	Date	Description
0.0	20 April 1998	Original
0.1	10 July, 1998	Page 22, added 55531C to the mask revision table, Page 26, t_{CDLY} changed from 30 to 40ns.
1.0	22 May, 2000	Upgraded to 70 MHz clock rate throughout Page 26, revised timing specifications: Fck, tDLY, tHD,tSSU, tSHD, tCDLY, Notes. Pages 34, 35, Changed Notes for diagnostics 3 and 4 Page 37, Corrected input test Table 17.

LIST OF FIGURES

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GC4114 DATASHEET

1.0 KEY FEATURES

- Four identical up-convert channels
- Independent modulation frequencies
- Independent phase/gain controls
- The four input signals are summed into a single output signal
- Maximum output rate of 70 MHz
- 16 bit real or complex inputs
- Interpolation factors of
  16 to 32,768 in the real input mode
  32 to 65,536 in the complex input mode
- Bit serial input format, or
- Memory mapped input registers
- 8 to 16 bit output samples
- 2's Complement or offset-binary output format
- 0.02 Hz tuning resolution
- 90 dB Spur Free Dynamic Range
- > 90 dB far image rejection
- > 70dB near image rejection
- 0.07 dB gain resolution
- 0.05 dB peak to peak passband ripple
- User programmable 63 tap input filter
- Accepts QPSK or QAM symbol data directly, performs transmit (pulse shape) filtering
- Meets Damps and GSM specifications
- Sum I/O path to merge outputs from multiple GC4114 chips
- Microprocessor interface for control, input, and diagnostics
- Built in diagnostics
- Microprocessor and serial inputs will accept either 3.3 or 5 volt input levels.
- 800 mW at 33 MHz, 3.3 volts
- 100 pin thin QFP package

2.0 BLOCK DIAGRAM

A block diagram illustrating the major functions of the chip is shown in Figure 1.

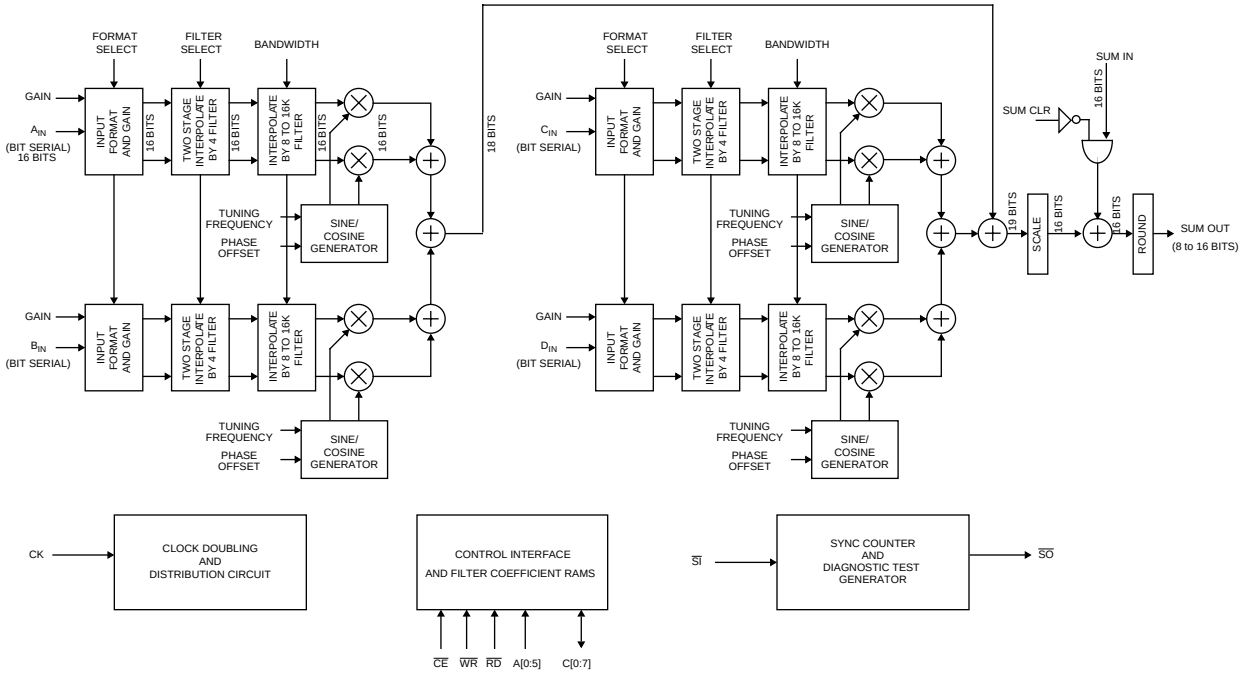


Figure 1. GC4114 Block Diagram

3.0 FUNCTIONAL DESCRIPTION

The GC4114 quad transmit chip contains four identical up-conversion circuits. Each up-convert circuit accepts a real or complex signal, interpolates it by a programmable factor ranging from 32 to 65,536 (16 to 32,768 for single-sideband modulation), up-converts the signal to a selected center frequency, sums it with other up-converted samples and outputs the combined signal. The chip contains a user programmable input filter which can be used to shape the transmitted data, or can be used as a Nyquist transmit filter for digital data transmission. See the application notes in Section 7.5 for details on using the chip to transmit QPSK or QAM data.

The up-converters are designed to maintain over 90 dB of spur free dynamic range and image rejection. Each up-convert circuit accepts 16 bit inputs (bit serial) and produces 16 bit outputs. The up-converter outputs are summed with an external 16 bit input to produce a single 16 bit output. The frequencies and phase offsets of the four sine/cosine sequence generators can be independently specified, as can the gain of each circuit. The up-converters share the same bandwidth, filter coefficients and input formats.

On chip diagnostic circuits are provided to simplify system debug and maintenance.

The chip receives configuration and control information over a microprocessor compatible bus consisting of an 8 bit data I/O port, a 6 bit address port, a chip enable strobe, a read strobe and a write strobe. The chip's 64 control registers (8 bits each) are memory mapped into the 6 bit address space of the control port.

3.1 CONTROL INTERFACE

The chip is configured by writing control information into sixty four control registers within the chip. The contents of these control registers and how to use them are described in Section 5. The registers are written to or read from using the **C[0:7]**, **A[0:5]**, $\overline{\textbf{CE}}$, $\overline{\textbf{RD}}$ and $\overline{\textbf{WR}}$ pins. Each control register has been assigned a unique address within the chip. This interface is designed to allow the GC4114 to appear to an external processor as a memory mapped peripheral (the pin $\overline{\textbf{RD}}$ is equivalent to a memory chip's $\overline{\textbf{OE}}$ pin).

An external processor (a microprocessor, computer, or DSP chip) can write into a register by setting **A[0:5]** to the desired register address, selecting the chip using the $\overline{\textbf{CE}}$ pin, setting **C[0:7]** to the desired value and then pulsing $\overline{\textbf{WR}}$ low. The data will be latched on the rising edge of $\overline{\textbf{WR}}$ or $\overline{\textbf{CE}}$.

To read from a control register the processor must set **A[0:5]** to the desired address, select the chip with the $\overline{\textbf{CE}}$ pin, and then set $\overline{\textbf{RD}}$ low. The chip will then drive **C[0:7]** with the contents of the selected register. After the processor has read the value from **C[0:7]** it should set $\overline{\textbf{RD}}$ and $\overline{\textbf{CE}}$ high. The **C[0:7]** pins are turned off (high impedance) whenever $\overline{\textbf{CE}}$ or $\overline{\textbf{RD}}$ are high or when $\overline{\textbf{WR}}$ is low. The chip will only drive these pins when both $\overline{\textbf{CE}}$ and $\overline{\textbf{RD}}$ are low and $\overline{\textbf{WR}}$ is high.

One can also ground the $\overline{\textbf{RD}}$ pin and use the $\overline{\textbf{WR}}$ pin as a read/write direction control and use the $\overline{\textbf{CE}}$ pin as a control I/O strobe.

Figure 2 shows timing diagrams illustrating both I/O modes.

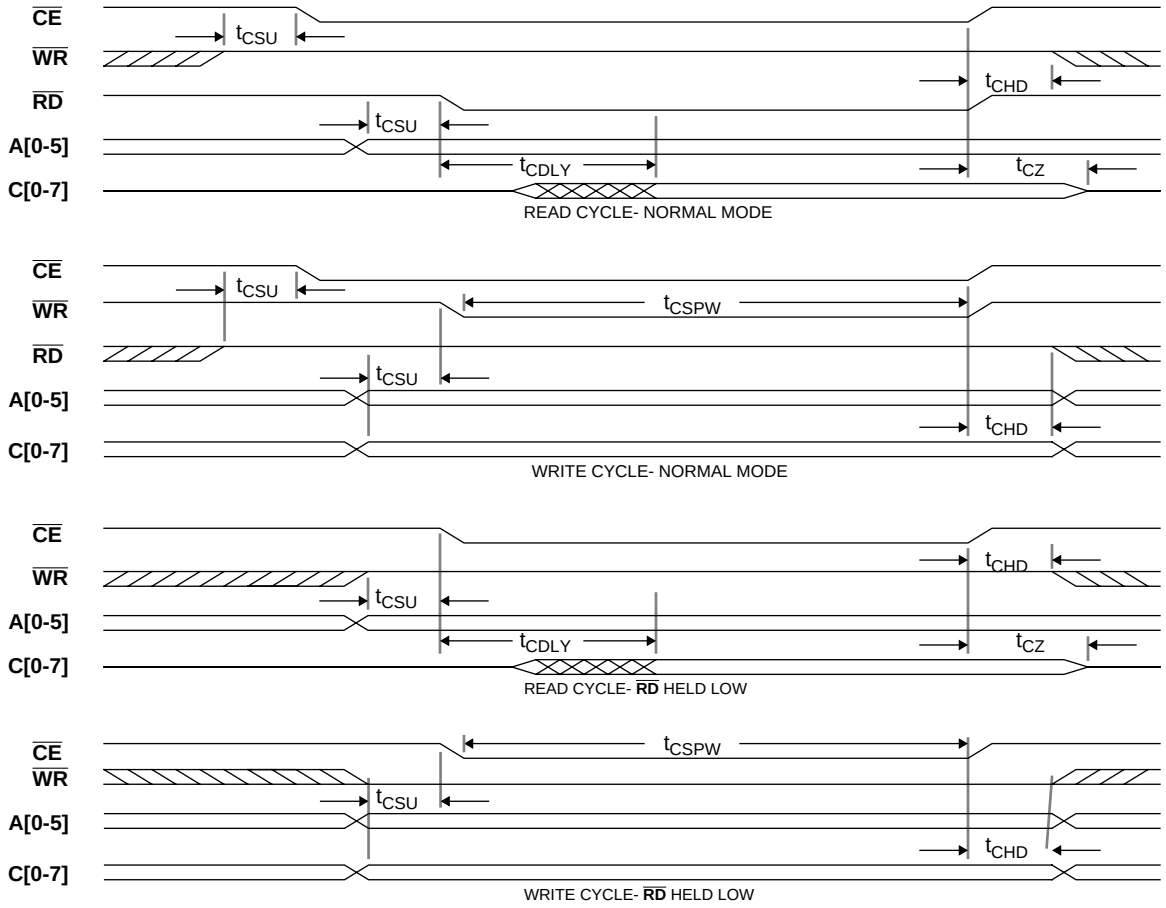


Figure 2. Control I/O Timing

The setup, hold and pulse width requirements for control read or write operations are given in Section 6.0.

The **C**, **A**, **$\overline{WR}$**, **$\overline{RD}$** and **$\overline{CE}$** pins will accept either 5 volt or 3.3 volt input levels. Separate power supply pins (**V_{UP}**) are provided on the chip to enable this feature.

3.2 INPUT FORMAT

The input samples are 16 bits, either real or complex, in 2's complement format. The samples are input to the chip either through the bit-serial input ports, or through memory mapped control registers.

3.2.1 Bit Serial Interface

The bit serial format consists of a data input pin, a bit clock pin, and a frame strobe pin for each of the four channels, and a data request pin which is common to all channels. The input accepts either individual 16 bit words in a format compatible with almost all DSP chips, or as the upper 16 bits of 32 bit words, or as two 16 bit words packed into a 32 bit word. The bit serial data is always entered MSB first. Complex values are entered I-half first followed by the Q-half, either as two separate transfers, or as a single 32 bit word with the I-half in the MSBs and the Q-half in the LSBs. Real values can be entered as 16 bit words or 32 bit words. In the 32 bit mode each 16 bit

real word is placed in the upper 16 bits of the 32 bits. Real samples can also be entered in the complex input mode by alternately placing samples in the I and Q halves of the complex input words. The data request signal (REQ) is output from the chip to identify when the GC4114 is ready for another serial input sample.

The bit serial inputs use the format shown in Figure 3:

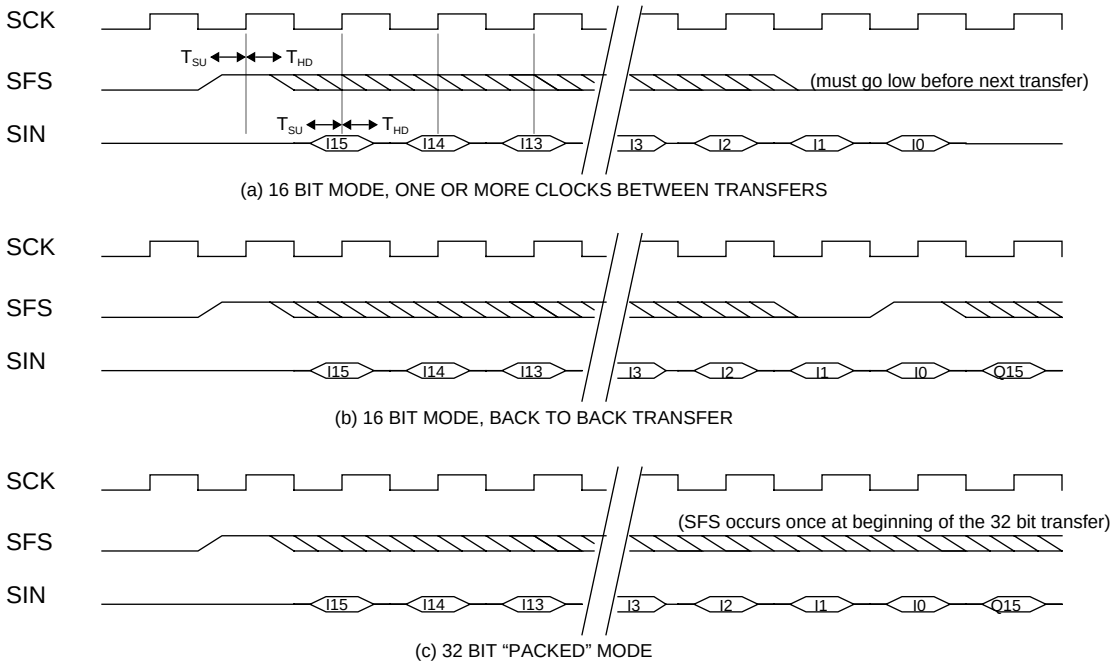


Figure 3. Serial Input Formats

Figure 3a shows the standard input mode (PACKED in the input control register is low). The user provides a bit serial clock (SCK), a frame strobe (SFS) and a data bit line (SIN). The chip clocks SFS and SIN into the chip on the rising edge of SCK (or falling edge if the SCK_POL bit in the input control register is set). The user sends a 16 bit serial input word to the GC4114 by setting SFS high (or low if SFS_POL in the input control register is set) for at least one SCK clock cycle, and then transmitting the data, MSB first, on the next 16 SCK clocks. The user must set SFS low at least one SCK clock cycle before the next serial transfer. The data can be transmitted "back to back" as shown in Figure 3b as long as the SFS signal toggles low and then high as shown. If the PACKED control bit is high, then the I and Q samples are sent as a single 32 bit word with only one SFS strobe as shown in Figure 3c.

The GC4114 input interface sends a "new sample request" strobe (REQ) when a new input sample is required for the up-converter channels. The input sample rate is $F_S=F_{CK}/2N$ for real inputs and $F_S=F_{CK}/4N$ for complex inputs, where F_{CK} is the chip's clock rate and N is the interpolation ratio in the CIC filter which varies from 8 to 16,384 (See Section 5.4). This means that the REQ strobe will be output from the chip every 2N clocks (CK, not SCK) in the real mode or every 4N clocks in the complex mode. The pulse width of the REQ strobe can be specified by the user to be either 2 clocks (CK) wide or N/2 clocks wide. The polarity of REQ is user programmable. The REQ strobe is typically used as an interrupt to an external device to tell it to send another input sample. The GC4114 chip must receive the last data bit at least one bit clock (SCK) period before the next REQ strobe.

If the serial interface timing is tight, i.e., the serial bit rate is so slow that the serial frames barely fit between REQ strobes, then the bit serial transfer can start up to 7 bit clocks before the REQ strobe. This means that the frame sync can be sent up to 7 bit clocks before REQ.

Very Important Note: The chip assumes that the serial clock is continuous, and does not stop between transfers. The SCK clock may stop, but must be active when frame sync occurs, and be active for one cycle after the last bit is sent. Serial data can be sent using only 32 bit clocks per REQ period if the frame sync for the 16 bit I word (or the 32 bit I/Q word in the PACKED mode) is synchronized to occur between 7 and 2 bit periods *before* REQ.

The user can choose to operate the serial lines as either 3.3 or 5 volt logic levels to facilitate the interface of the GC4114 chip with external circuitry.

3.2.2 Memory Mapped Interfaced

Input samples can be entered into the chip using the control interface. Addresses 16 through 31 are the input data registers. Note that these registers can be written to in a DMA burst, 8 bits at a time. Note that some DMA formats write samples most significant byte first. If this is the case then the DMA should write from address 31 down to address 16. The REQ strobe from the GC4114 chip defines when the DMA transfer can start. The transfer must be done before the next REQ strobe is received.

3.3 GAIN

Each input sample is multiplied by an 8 bit 2's complement gain word. If the gain word is 'G', which ranges from -128 to +127, then the gain adjustment will be G/128. This gives a 42 dB gain adjustment range. Setting G to zero clears the channel. A different gain can be specified for each channel. Gain is described in more detail in Section 3.7.

3.4 THE UP-CONVERTERS

Each up-converter channel uses a two stage interpolate by four filter and a 4 stage cascaded integrate-comb (CIC) filter to increase the sample rate of the input data up to a sample rate equal to the chip's clock rate. An NCO and mixer circuit to modulate the signal up to the desired center frequency. A block diagram of each up-convert channel is shown below:

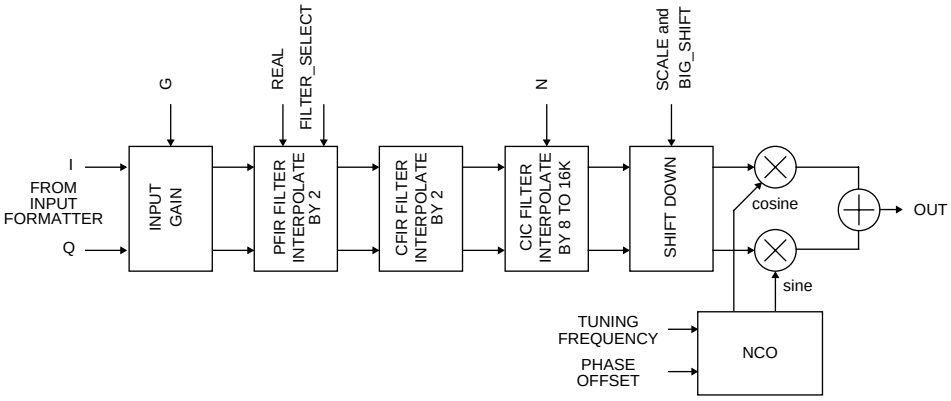


Figure 4. The Up-converter Channel

After the gain has been applied, as described in the previous section, the input data is interpolated by a factor of 2 in a 63 tap filter with programmable coefficients (PFIR). The user can choose between an internal default filter shape for the PFIR, or can download a custom set of taps. A typical use of the user down loaded coefficients is to implement matched (root-raised-cosine) transmit filters.

The PFIR will also, if desired, convert real input data to single-sideband complex data. In this mode the PFIR does not interpolate by a factor of 2. Instead it down-converts the input data by $F_S/4$, where F_S is the input sample rate, and low pass filters the result.

The second interpolate by 2 filter is a 31 tap compensating filter (CFIR) which pre-compensates for the droop associated with the CIC filter that follows it.

The CIC filter interpolates by another factor of N=8 to 16,384 to give an overall interpolation factor of 32 to 65,536 (16 to 32,768 in the real input mode).

The interpolated signal is up-converted by a sine/cosine sequence generated by the NCO. The real part (I-half) of the complex result is saved as the channel output.

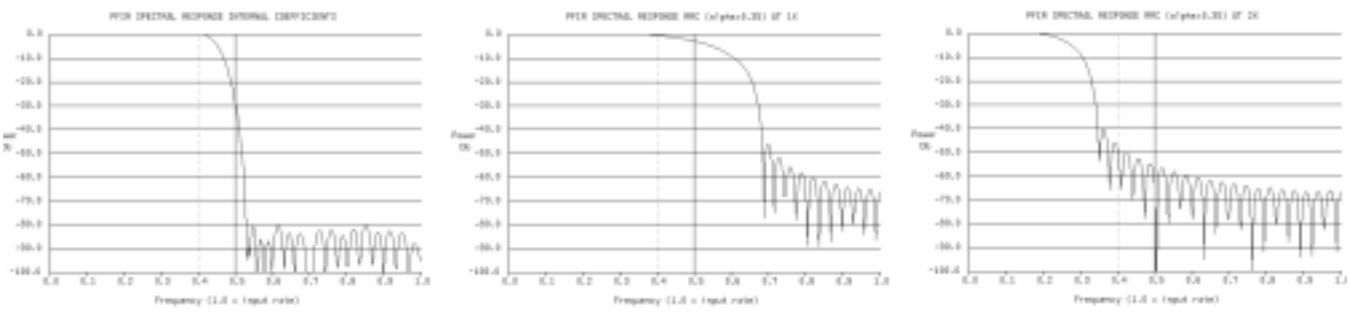
3.4.1 The Programmable Input Filter (PFIR)

The programmable input filter uses either internal ROM based coefficients, or externally downloaded filter coefficients. The 63 filter coefficients are quantized to 16 bit words. The internal 80% bandwidth filter is flat over the range of $-0.4F_S$ to $+0.4F_S$ with 0.03 dB of passband ripple, and with 80db of out of band image rejection. The 32 unique coefficients in the 63 tap symmetric filter are:

```
-14, -20, 19, 73, 43, -70, -82, 84, 171, -49, -269, -34, 374, 192, -449,
-430, 460, 751, -357, -1144, 81, 1581, 443, -2026, -1337, 2437, 2886,
-2770, -6127, 2987, 20544, 29647
```

The internal filter is typically used for signals that are digitized analog signals such as voice, AM, FM or SSB signals. The internal filter is also used for digital signals (FSK, PSK, QAM or GMSK signals for example) that have already been modulated and filtered and are ready to be up-converted to their desired carrier frequency.

The external coefficients are typically used to “pulse shape” and then up-convert digital data. The PFIR will accept QPSK, O-QPSK, PSK, PAM, OOK, π/4-QPSK, or QAM symbols and then filter them by the desired pulse shaping filter. A common pulse shaping filter is the root-raised-cosine (RRC) filter. The symbols can be entered directly into the chip at the desired symbol (baud) rate, or entered at twice the baud rate by alternately entering symbol data and entering zeroes.[1] The “twice the baud rate” or “2X” method results in better out of band image rejection. See the application note in Section 7.5 for more details.



(a) Internal Coefficients (b) RRC (Alpha=0.35) Filter (c) RRC (Alpha=0.35) At 2X

Figure 5. PFIR Spectral Response

Figure 5a shows the spectral response of the internal filter. Figure 5b shows the root-raised-cosine pulse shaping filter with 35% excess bandwidth (alpha=0.35). Figure 5c shows the RRC shape for the 2X mode.

1. Called zero padding.

The set of coefficients used to generate the RRC filter shown in Figure 5b are:

```
27, -20, -6, 34, -30, -9, 39, -37, -1, 52, -55, -5, 62, -72, 15, 92,
-117, 8, 112, -175, 82, 224, -348, 61, 286, -761, 766, 1708, -4042,
-2533, 18177, 32767
```

The set of coefficients used to generate the 2X RRC filter shown in Figure 5c are:

```
-12, -117, -113, 8, 127, 112, -38, -175, -134, 82, 275, 224, -71,
-348,-307, 61, 398, 286, -286, -761, -442, 766, 1954, 1708, -660,
-4042,-5641, -2533, 6187, 18177, 28625, 32767
```

The PFIR will accept either complex or real input data. If the input samples are complex, the filter doubles the input rate by inserting zeroes between each sample, and then low pass filtering the result. If the input samples are real, the filter translates the real samples down by $F_S/4$, where F_S is the input sample rate, by multiplying them by the complex sequence +1, -j, -1, +j, …, and then lowpass filtering the result. This generates a single-sideband modulation of the real input. If double sideband real upconversion is desired, then the chip should be operated in the complex mode with the Q-half of each complex pair set to zero.

The PFIR has a gain which is equal to (PFIR_SUM/65536), where PFIR_SUM is equal to the sum of all of the filter coefficients. The internal filter coefficients have PFIR_SUM=65543 which gives very close to unity gain. The RRC filter shown in Figure 5b has PFIR_SUM=59821 and the 2X RRC filter shown in Figure 5c has PFIR_SUM=119357. See Section 3.7 for more details on the chip's gain settings.

The PFIR output rate relative to the input rate is $2F_S$ in the complex input mode and is F_S in the real (single side band) mode. The output rate relative to the clock rate is $F_{CK}/2N$.

3.4.2 The Compensating Interpolate by 2 Filter (CFIR)

The second stage filter is a fixed coefficient 31 tap interpolate by 2 filter. The second stage filter always interpolates by a factor of two. The second filter has a passband which is flat (0.01 dB ripple) over 100% of the input bandwidth ($-0.5F_S$ to $+0.5F_S$). The second filter also compensates for the droop associated with the CIC interpolation filter described in the next section. The 16 unique coefficients of the symmetric filter are:

```
-23, -3, 103, 137, -21, -230, -387, -235, 802, 1851, 81, -4372, -4774,
5134, 20605, 28216
```

The CFIR output is scaled to have unity gain. The output rate of the CFIR filter is $4F_S$ in the complex mode and is $2F_S$ in the real mode. The CFIR output rate relative to the clock rate is F_{CK}/N.

3.4.3 The CIC Interpolate by N Filter

The CFIR output is interpolated by a factor of N in the CIC[1] filter, where N is any integer between 8 and 16,384. The filter is a 4 stage CIC filter. A block diagram of the CIC filter is shown in Figure 6.

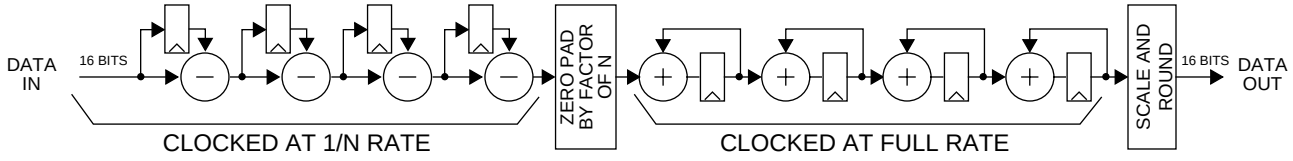


Figure 6. Four Stage CIC Interpolate by N Filter

1. Hogenauer, Eugene B., An Economical Class of Digital Filters for Decimation and Interpolation, IEEE transactions on Acoustics, Speech and Signal Processing, April 1981.

The output of the CIC interpolation filter is equal to the clock rate. The CIC filter has a gain equal to N^3 which must be removed by the "SCALE AND ROUND" circuit shown in Figure 6. This circuit has a gain equal to $2^{-(3+SCALE+12*BIG\_SHIFT)}$, where SCALE ranges from 0 to 15 and BIG_SHIFT ranges from 0 to 2. The value chosen for BIG_SHIFT must also satisfy: $2^{(12*BIG\_SHIFT+18)} \geq N^3$. Overflows due to improper gain settings will go undetected if this relationship is violated. This restriction means that BIG_SHIFT = 0 for N between 8 and 64, BIG_SHIFT = 1 for N between 65 and 1024, and BIG_SHIFT = 2 for N between 1025 and 16384.

The CIC filter must be initialized when the chip is first configured or whenever the interpolation value N or the shift value BIG_SHIFT are changed. The CIC filter is initialized using the flush controls described in Section 5.8. If the CIC is disturbed during processing due to noise, radiation particles, or due to changing N or BIG_SHIFT, then it will become unstable and generate wideband white noise in the output. This instability can be prevented by using the "auto flush" capability of the chip[1] (See control register 2, bit 6 in Section 5.3). The auto flush mode detects the CIC instability and automatically re-initializes the CIC. The auto flush mode requires that the gain up to the output of the CIC filter is less than or equal to unity.

3.4.4 The Sine/Cosine Generator

The tuning frequency of each up-converter is specified as a 32 bit word and the phase offset is specified as a 16 bit word. The tuners can be synchronized with tuners on other chips. This allows multiple up-converter outputs to be coherently combined, each with a unique phase and amplitude. A block diagram of the NCO (Numerically Controlled Oscillator) circuit is shown in Figure 7.

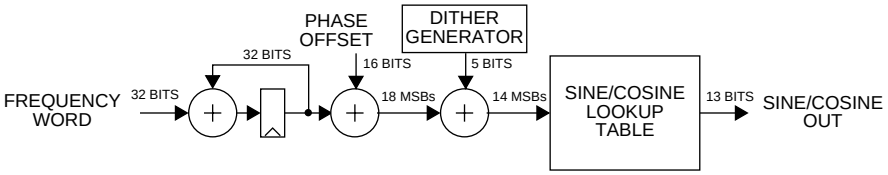


Figure 7. NCO Circuit

The NCO's spur level is reduced to below 90 dB through the use of phase dithering. Figure 8 shows an example NCO output with and without dithering. Notice that the spur level without dithering is about -82 dB, and the spur level with dithering is well below -90 dB.

The tuning frequency is set according to the formula $FREQ = 2^{32}F/F_{CK}$, where F is the desired tuning frequency and F_{CK} is the chip's clock rate. The 16 bit phase offset setting is $PHASE = 2^{16}P/2\pi$, where P is the desired phase in radians ranging between 0 and 2π

1. The auto flush mode is a patent pending feature of the chip.

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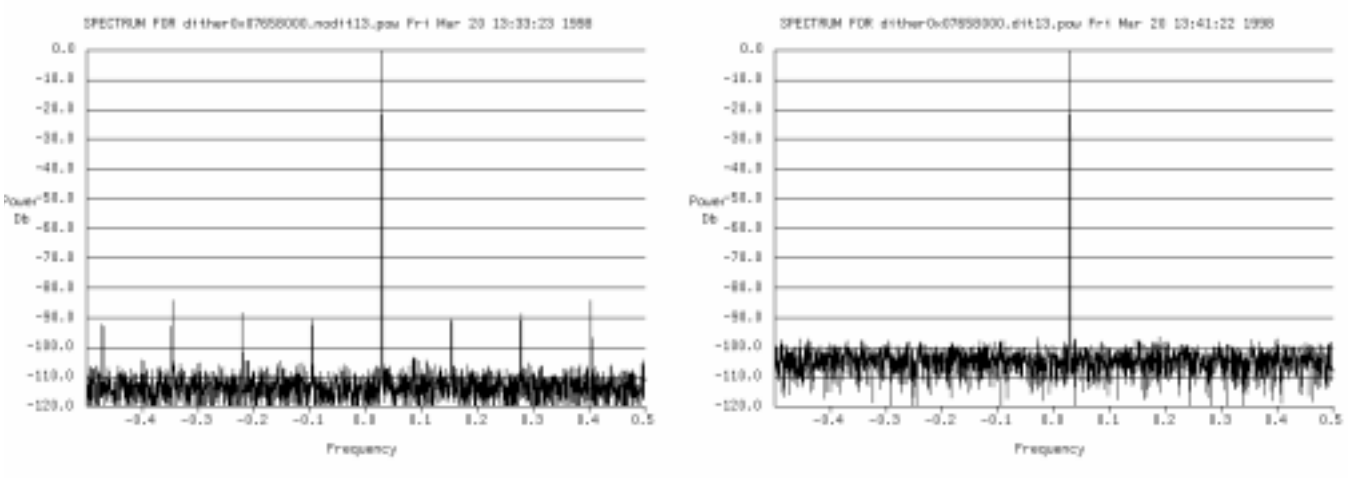
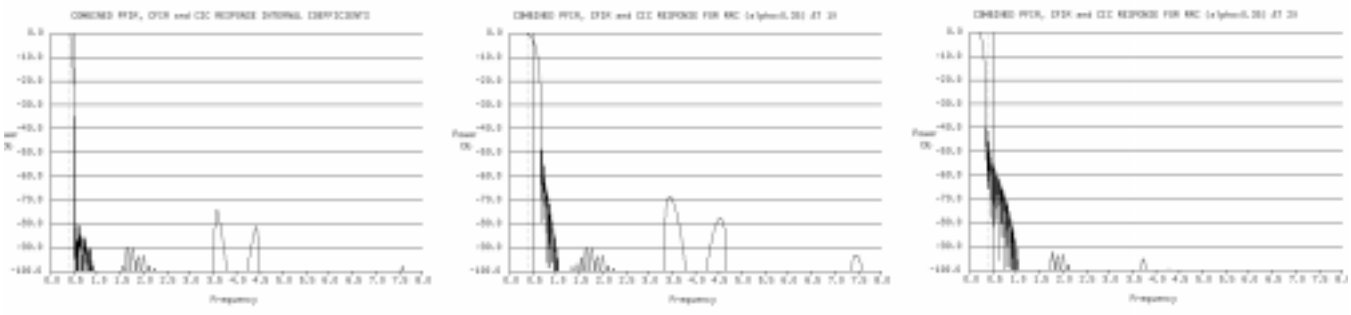


No Dithering With Dithering

Figure 8. Example NCO Output

3.5 THE OVERALL INTERPOLATION FILTER RESPONSE

The image rejection of the up-convert channel is equal to the stop band rejection of the overall interpolation filter response. The overall response is obtained by superimposing the interpolated responses of the PFIR and CFIR filters onto the CIC filter response. The overall response is shown in Figure 9. Figure 9a shows the overall response using the default PFIR coefficients. Figure 9b shows the response using a root-raised-cosine PFIR coefficient set. Figure 9c shows the response when using the 2x mode root-raised cosine PFIR coefficient set.



(a) Internal Coefficients (b) RRC (Alpha=0.35) Filter (c) RRC (Alpha=0.35) At 2X

Figure 9. Overall Filter Response

3.6 THE SUM TREE

The four up-convert channel outputs are summed together, scaled down by powers of two and then added to an external sum input. The sum tree output is rounded to 8, 10, 12, 14 or 16 bits and output from the chip. The sum of the four channels within the chip can be scaled down by powers of two in order to prevent saturation when channels from multiple chips are summed together. The scale factor is equal to 2^{-SUM_SCALE}, where SUM_SCALE is 0,1,2 or 3 (See Section 5.9). Overflows in the sum tree are saturated to plus or minus full scale.

The latency from IN[0:15] to OUT[[0:15] is seven clock cycles. The chip will optionally invert the MSB output (OUT15) from the chip in order to drive offset binary format digital to analog converters (DACs)

3.7 OVERALL GAIN

The overall gain of the chip is a function of the sum of the programmable filter coefficients (PFIR_SUM) described in Section 3.4.1, the amount of interpolation in the CIC filters (N described in Section 3.4.3), the scale circuit settings in the CIC filter (SCALE and BIG_SHIFT described in Section 3.4.3), and the sum tree scale factor (SUM_SCALE described in Section 3.6). The overall gain is:

$$\text{GAIN} = \left\{\frac{\text{G}}{128}\right\}\left\{\frac{\text{PFIR\_SUM}}{65536}\right\}\{\text{N}^3 2^{-(\text{SCALE} + 12 \times \text{BIG\_SHIFT} + 3)}\}\{\ 2^{-\text{SUM\_SCALE}}\}$$

where G can be different for each channel, but N, SCALE, BIG_SHIFT, SUM_SCALE and PFIR_SUM are common to all channels.

The optimal gain setting is one which will keep the amplitude of the data within the channel as high as possible without causing overflow. The recommended gain target is to keep the root-mean-squared amplitude of the data close to one-fifth (0.2) full scale (a 14 dB crest factor). This level should be maintained throughout the channel computations. This means that the products $\left\{\frac{\text{RMS}}{32768}\right\}\left\{\frac{\text{G}}{128}\right\}\left\{\frac{\text{PFIR\_SUM}}{65536}\right\}$ and $\left\{\frac{\text{RMS}}{32768}\right\}\left\{\frac{\text{G}}{128}\right\}\left\{\frac{\text{PFIR\_SUM}}{65536}\right\}\{\text{N}^3 2^{-(\text{SCALE} + 12 \times \text{BIG\_SHIFT} + 3)}\}$ should both be less than or equal to 0.2, where “RMS” is the root-mean-squared level of the input data. Other crest factors can be used depending upon the application. For example, a crest factor of 12 dB is adequate if the final number of bits going to a DAC is 12 bits. In most cases the input data will already have the correct crest factor for the application, in which case the ratio $\left\{\frac{\text{RMS}}{32768}\right\}$ will be equal to the crest factor (e.g., 0.2) and the gain settings in the channel should be set to unity.

The sum tree gain (SUM_SCALE) is used when the outputs from multiple channels are summed together. The recommended gain when “M” uncorrelated channels are being added together is $\frac{1}{\sqrt{M}}$. For example, if all four channels are active in a GC4114, then M is four and the gain should be 1/2, which can be achieved by setting SUM_SCALE equal to 1. If four chips are cascaded to sum sixteen channels, then M is 16 and the gain should be 1/4, which implies SUM_SCALE should be 2.

The $\frac{1}{\sqrt{M}}$ gain rule assumes that the channels can be treated as uncorrelated signals which will result in an average amplitude gain of $\sqrt{M}$. If the signals are correlated, however, the amplitude gain can be M and the sum tree gain should be set to $\frac{1}{M}$. Examples of correlated signals are pure tones or modem signals that have been synchronized so that they might peak at the same time. These signals, however, require a much smaller crest factor, such as 3 dB for pure tones and 6 dB for modem signals. In this case the crest factor of 14 dB will absorb much of the difference in gain between $\sqrt{M}$ and M.

If overflow does occur, then the samples are saturated to plus or minus full scale. Overflow can be monitored using the overflow status register, see Section 5.14 for details.

The values of N and BIG_SHIFT must also satisfy $2^{(12*\text{BIG\_SHIFT}+18)} \geq \text{N}^3$ (see Section 3.4.3 for details). If N and BIG_SHIFT do not satisfy this relationship, then an overflow may occur which may not be detected.

If the auto flush mode is used, then the gain in the CIC must be less than or equal to unity. This means that the values of N, SCALE and BIG_SHIFT must satisfy $2^{(\text{SCALE}+12*\text{BIG\_SHIFT}+3)} \geq \text{N}^3$ (see Section 3.4.1 for details).

Note that noise due to rounding errors is minimized by keeping the gain as close to unity as is possible. If attenuation is necessary, for example when multiple channel outputs are to be added together, then the attenuation should be added as close to the output of the chip as is possible. This means that the SUM_SCALE control should be used to add attenuation before the SCALE and BIG_SHIFT controls are adjusted.

3.8 CLOCKING

The chip can be clocked in one of two modes. In the standard mode, the clock rate is equal to the output data rate which can be up to 70 MHz. An internal clock doubler doubles the clock rate so that the internal circuitry is clocked at twice the data rate. To use the standard mode the CKMODE pin must be grounded and the internal control register bit EN_DOUBLER must be set high (See Section 5.10).

The alternate clock mode (pin CKMODE is high) accepts a double rate clock on the CK2X pin and bypasses the clock doubler circuit. The EN_DOUBLER control bit should be low. In the alternate mode the user must provide both the standard clock and the double rate clock. Note that the rising edges of the two clocks must be such that the rising edge of CK is coincident with or precedes the rising edge of CK2X by no more than 2 nanoseconds.

3.9 SYNCHRONIZATION

Multiple chips can be synchronized through the use of a sync input signal, an internal one shot sync generator, and a sync counter. Each circuit within the chip, such as the sine/cosine generators or the interpolation control counter can be synchronized to one of these sources. These syncs can also be output from the chip so that multiple chips can be synchronized to the sync coming from a “master” chip. See Figure 10 in Section 7.5.

The interpolation control counter generates the request strobe (REQ) output from the chip. This counter can be syncronized using the input $\overline{SI}$ sync (see bits 2 and 3 of address 0). This allows the user to lock the timing of the request strobe to the $\overline{SI}$ timing. If this is done, then the REQ strobe will go high 5 clock cycles after the $\overline{SI}$ signal. For example, if the $\overline{SI}$ signal is active during clock cycle 0, then REQ will go high during clock cycle 5 and then repeat every 4N clocks (or 2N clocks in the real input mode) thereafter.

3.10 POWER DOWN MODES

The chip has a power down circuit. This circuit contains a slow, nominally 1 KHz, oscillator and a clock-loss detect cell. This circuit is used to detect the loss of clock and provide a slow “keep-alive” clock to the chip. The circuit is also used to power down the chip by switching from the high speed input clock to the low speed keep-alive clock. The low speed clock rate is slow enough to power down the chip while fast enough to refresh the dynamic nodes within the chip. The user can select whether this circuit is in the automatic clock-loss detect mode, is always on (power down mode), or is disabled (the slow clock never kicks in).

3.11 DIAGNOSTICS

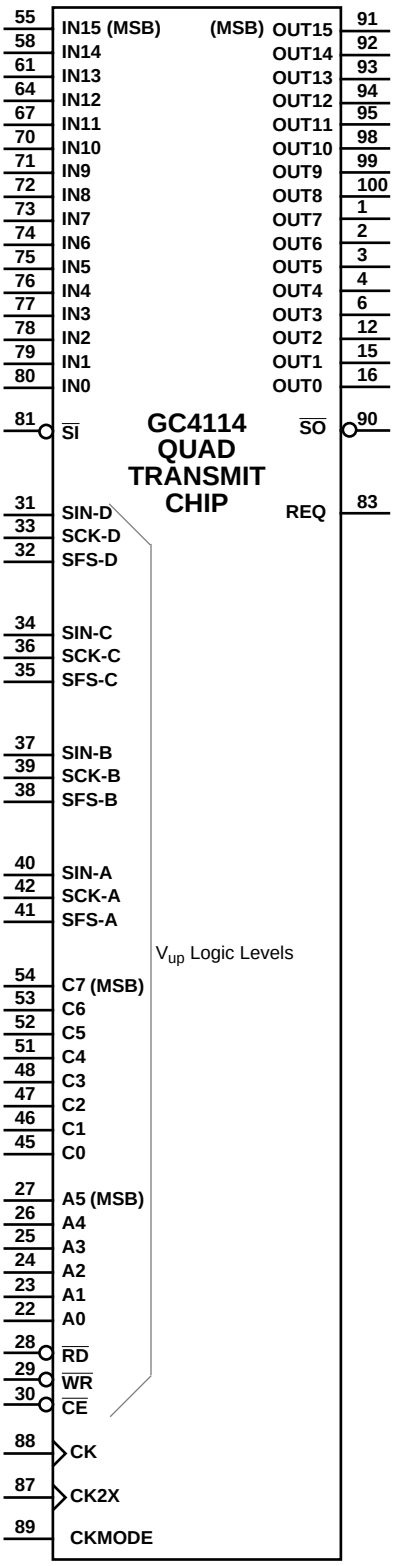
The chip has an internal ramp generator which can be used in place of the data inputs for diagnostics. An internal checksum circuit generates a checksum of the output data to verify the chip’s operation. See Section 7.6 for diagnostic configurations and checksums.

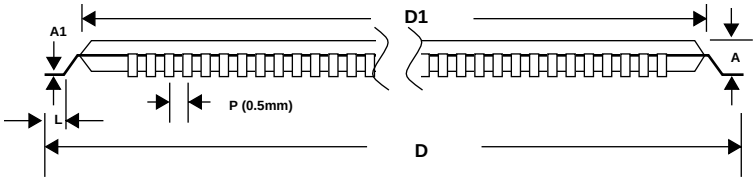
3.12 INITIAL BOARD DEBUG PROCEDURE

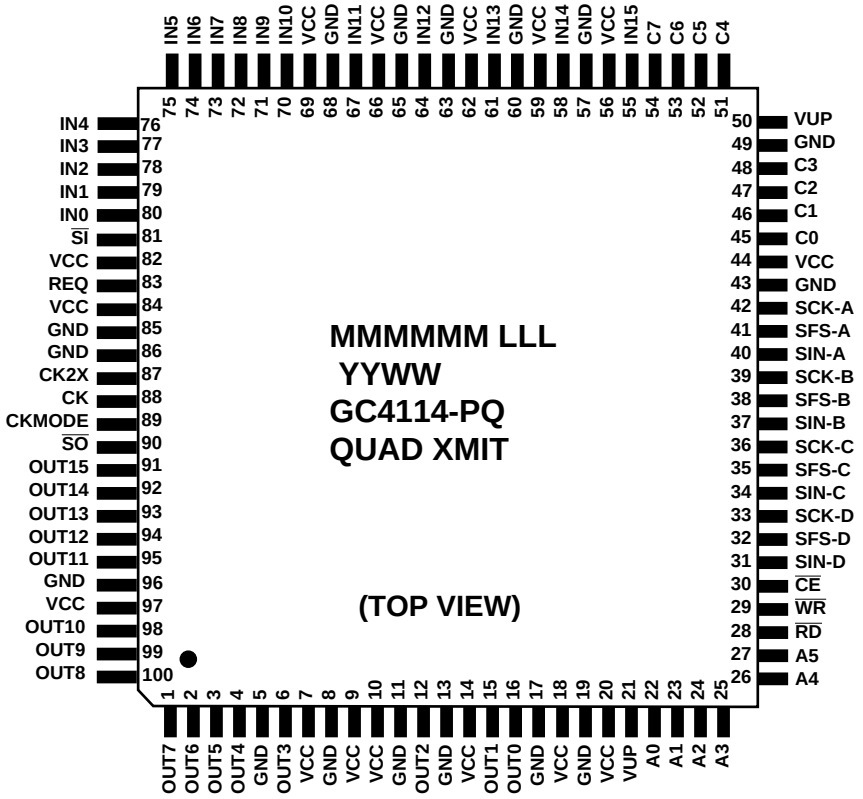
The suggested procedure for bringing up the GC4114 chip is to first check the control interface by writing to the control registers and reading them back. The diagnostics described in Section 7.6 should be run next, followed by the output and input tests described in Sections 7.7 and 7.8. If these pass successfully, then the configuration customized for the desired application should work.

4.0 PACKAGING

The GC4114 chip comes in a 100 pin thin plastic quad flatpack package







100 PIN THIN QUAD FLAT PACK
GC4114-PQ: PLASTIC PACKAGE
GC4114-CQ: CERAMIC PACKAGE

DIMENSION		PLASTIC	CERAMIC
D	(width pin to pin)	16.0 mm (0.630")	17.2 mm (0.677")
D1	(width body)	14.0 mm (0.551")	14.0 mm (0.551")
P	(pin pitch)	0.5 mm (0.020")	0.5 mm (0.020")
B	(pin width)	0.22 mm (0.009")	0.20 mm (0.008")
L	(leg length)	0.60 mm (0.024")	0.70 mm (0.028")
A	(height)	1.5 mm (0.059")	3.1 mm (0.122")
A1	(pin thickness)	0.15 mm (0.006")	0.2 mm (0.008")

MMMMM = Mask Code
LLL = Lot Code
YYWW = Date Code

VCC PINS:7,9,10,14,18,20,44,56,59,62,66,69,82,84,97

GND PINS:5,8,11,13,17,19,43,49,57,60,63,65,68,85,86,96

VUP PINS: 21, 50

NOTE: 0.01 to 0.1 µf DECOUPLING CAPACITORS SHOULD BE PLACED AS CLOSE AS POSSIBLE TO EACH SIDE OF THE CHIP

SIGNAL	DESCRIPTION
SIN-A,B,C,D	**BIT SERIAL INPUT DATA,** *Active high* The bit serial input data for the four channels. The I and Q halves of complex data are entered on the same pin. Each time the chip asserts **REQ** (See below) the I-half is entered and then the Q-half.
SCK-A,B,C,D	**BIT SERIAL DATA CLOCK**, *Active high or low* The serial data bits are clocked into the chip by these clocks. The active edge of these clocks are user programmable.
SFS-A,B,C,D	**BIT SERIAL FRAME STROBE**, *Active high or low* The bit serial word strobe. This strobe delineates the 16 bit words within the bit serial input stream. This strobe can be a pulse at the beginning of each bit serial word, or can act as a window enable which is active while the data bits are active.
REQ	**REQUEST FLAG**, *programmable active high or low* The chip requests new input data by asserting this signal. The width in input clock cycles and polarity of this signal are user programmable. This signal is typically used as an interrupt to a DSP chip, but can also be used as a start pulse to dedicated circuitry.
CK	**INPUT CLOCK.** *Active high* The clock input to the chip. The **IN[0:15]** and $\overline{\textbf{SI}}$ input signals are clocked into the chip on the rising edge of this clock.
CK2X	**DOUBLE RATE INPUT CLOCK.** *Active high* The double rate clock input to the chip. Used in the alternate clock mode to clock the chip. This clock must be exactly twice the frequency of the **CK** clock. Should be grounded in the normal clock mode.
CKMODE	**CLOCK MODE,** *Active high* The clock mode control. The chip uses **CK2X** when this pin is tied high (alternate mode) to clock the internal circuitry. When this signal is grounded (normal mode) the chip doubles the **CK** clock to use as the internal clock.
$\overline{\textbf{SI}}$	**SYNC IN**. *Active low* The sync input to the chip. All timers, accumulators, and control counters are, or can be, synchronized to $\overline{\textbf{SI}}$. This sync is clocked into the chip on the rising edge of the input clock (**CK**).
$\overline{\textbf{SO}}$	**SYNC OUT**. *Active low* This signal is either a delayed version of the input sync $\overline{\textbf{SI}}$, the sync counter's terminal count (TC), or a one-shot strobe. The $\overline{\textbf{SO}}$ signal is clocked out of the chip on the rising edge of the input clock (**CK**).
IN[0:15]	**SUMMER INPUT DATA.** *Active high* The 16 bit two's complement summer input samples. New samples are clocked into the chip on the rising edge of the clock. The input data rate is assumed to be equal to the clock rate.
OUT[0:15]	**SUMMER OUTPUT DATA**. *Active high* The summer data are output as a 16 bit words on these pins. The bits are clocked out on the rising edge of the clock (**CK**).
C[0:7]	**CONTROL DATA I/O BUS**. *Active high* This is the 8 bit control data I/O bus. Control register data is loaded into the chip or read from the chip through these pins. The chip will only drive these pins when $\overline{\textbf{CE}}$ is low and $\overline{\textbf{RD}}$ is low.
A[0:5]	**CONTROL ADDRESS BUS**. *Active high* These pins are used to address the control registers within the chip. Each of the control registers within the chip are assigned a unique address. A control register can be written to or read from by setting **A[0:5]** to the register's address.
$\overline{\textbf{RD}}$	**READ ENABLE**. *Active low* This pin enables the chip to output the contents of the selected register on the **C[0:7]** pins when $\overline{\textbf{CE}}$ is also low.
$\overline{\textbf{WR}}$	**WRITE ENABLE**. *Active low* This pin enables the chip to write the value on the **C[0:7]** pins into the selected register when $\overline{\textbf{CE}}$ is also low.
$\overline{\textbf{CE}}$	**CHIP ENABLE**. *Active low* This control strobe enables the read or write operation. The contents of the register selected by **A[0:5]** will be output on **C[0:7]** when $\overline{\textbf{RD}}$ is low and $\overline{\textbf{CE}}$ is low. If $\overline{\textbf{WR}}$ is low and $\overline{\textbf{CE}}$ is low, then the selected register will be loaded with the contents of **C[0:7].**
VUP	**MICROPROCESSOR INTERFACE VOLTAGE**. This pin is used to set the voltage interface levels for the following control pins: **C[0:7]**, **A[0:5],** $\overline{\textbf{CE}}$**,** $\overline{\textbf{RD}}$**,** $\overline{\textbf{WR}}$, **SIN-A, SIN-B, SIN-C, SIN-D, SCK-A, SCK-B, SCK-C, SCK-D, SFS-A, SFS-B, SFS-C,** and **SFS-D**. This pin can be tied to +5 volts to interface the GC4114 to microprocessors with TTL outputs. Tie this pin to +3.3 volts (**VCC**) to interface with 3.3 volt microprocessors.

5.0 CONTROL REGISTERS

The chip is configured and controlled through the use of eight bit control registers. These registers are accessed for reading or writing using the control bus pins (**$\overline{CE}$**, **$\overline{RD}$**, **$\overline{WR}$**, **A[0:5]**, and **C[0:7]**) described in the previous section. The register names and their addresses are:

The Mode and Control Registers are addresses 0 to 15

ADDRESS	NAME	ADDRESS	NAME
0	Sync Mode	8	Channel A Sync
1	Interpolation Mode	9	Channel B Sync
2	Interpolation Gain	10	Channel C Sync
3	Interpolation Byte 0	11	Channel D Sync
4	Interpolation Byte 1	12	Channel Flush Mode
5	Input Mode	13	Summer Mode
6	Counter Byte 0	14	Status
7	Counter Byte 1	15	Checksum

The Input registers are addresses 16 to 31. The 16 bit inputs are stored least significant byte in the first address, the most significant in the second.

ADDRESSES	NAME	ADDRESSES	NAME
16,17	Channel A, I-input	24,25	Channel C, I-input
18,19	Channel A, Q-input	26,27	Channel C, Q-input
20,21	Channel B, I-input	28,29	Channel D, I-input
22,23	Channel B, Q-input	30,31	Channel D, Q-input

Addresses 32 to 63 are used in four modes as determined by the page select control bits in the status register. Page zero is the frequency, phase and gain settings for the four channels. Page one is for monitoring status and test points. Pages two and three are used to store the coefficients for the programmable interpolate by two filter.

The Page zero register assignments are:

ADDRESSES	NAME	ADDRESSES	NAME
32,33,34,35	Channel A Frequency	48,49,50,51	Channel C Frequency
36,37	Channel A Phase	52,53	Channel C Phase
38	Channel A Gain	54	Channel C Gain
39	unused	55	unused
40,41,42,43	Channel B Frequency	56,57,58,59	Channel D Frequency
44,45	Channel B Phase	60,61	Channel D Phase
46	Channel B Gain	62	Channel D Gain
47	unused	63	unused

The 32 fir filter coefficients are stored as two bytes per 16 bit word in 2's complement format. The least significant 8 bits in the lower byte and the most significant 8 bits in the upper byte. Page two stores coefficients 0 through 15 in addresses 32 to 63. Page three stores coefficients 16 to 31. Coefficient 31 is the center tap. The lower byte of the coefficient must be loaded and then the upper byte.

The following sections describe each of these registers. The type of each register bit is either R, W, or R/W indicating whether the bit is read only, write only, or read/write. All bits are active high.

5.1 SYNC MODE REGISTER

The Sync mode control register determines how the circuits within the chip are synchronized. Each circuit which requires synchronization can be configured to be synchronized to the sync input **(SI**), or to the terminal count of the sync counter (**TC**). The sync to each circuit can also be set to be always on or always off. Each circuit is given a two bit sync mode control which is defined as:

Table 1: Sync Modes

MODE	SYNC DESCRIPTION
0	“0” (never asserted)
1	SI
2	TC (or OS, if USE_ONESHOT is set)
3	“1” (always)

NOTE: the internal syncs are active high. The **$\overline{\text{SI}}$** input has been inverted to be the active high sync **SI**.

ADDRESS 0: **Sync Mode**, *suggested default = 0x65*

BIT	TYPE	NAME	DESCRIPTION
0,1 (LSBs)	R/W	INT_SYNC	Synchronizes the interpolation control counter. The interpolation counter controls the filtering of each channel.
2,3	R/W	COUNTER_SYNC	Synchronizes the sync counter. This counter is used to generate the periodic “TC” sync pulses. Mode 2 is OS, not TC, for the counter.
4,5	R/W	OUTPUT_SYNC	The selected sync is inverted and output on the **$\overline{\text{SO}}$** pin.
6	R/W	USE_ONESHOT	The terminal count mode in Table 1 is replaced by the one shot pulse (OS) when this bit is set.
7	R/W	ONE_SHOT	The one shot sync pulse (OS) is generated when this bit is set. This bit must be cleared before another one shot pulse can be generated.

If the user wishes to allow the chip to free run, asynchronous to other chips, then the sync settings can be set to zero. If one wishes to synchronize several chips to a single sync source, then the sync mode selections should be set to one. The suggested default is to output the one-shot (USE_ONESHOT = 1, OUTPUT_SYNC=2) and all other syncs to SI. The user should tie the **$\overline{\text{SO}}$** output pin of one GC4114 chip to the **$\overline{\text{SI}}$** input pin of all other GC4114 chips in a system in order to cleanly synchronize and initialize one or more GC4114 chips. If there is only a single GC4114 chip, then all sync mode selections can be set to “2” to receive the one-shot directly. A one-shot should be sent after initialization and each time the interpolation ratio is changed.

5.2 INTERPOLATION MODE REGISTER

Registers 1 and 2 control the interpolation modes for the chip. These settings are common to all channels

ADDRESS 1: **Interpolation Mode**, *suggested default = 0x00*

BIT	TYPE	NAME	DESCRIPTION
0 LSB	R/W	REAL	The input samples are real when this bit is set and are up-converted as a single sideband signal. The input samples are treated as complex when this bit is low. The input rate is $F_{CK}/4N$ when this bit is low and is $F_{CK}/2N$ when this bit is high, where F_{CK} is the chip's clock rate and N is the interpolation setting in registers 3 and 4 (See Section 5.4). If double sideband real data is to be up-converted, then the complex mode should be used with the Q-half set to zero.
1	R/W	FILTER_SELECT	The user downloaded filter coefficients are used instead of the built in filter coefficients for the PFIR filter when this bit is set. This bit must be cleared for at least 4N clock cycles before it is set.
2	R/W	REQ_POL	This control bit inverts the polarity of the **REQ** output. Normally **REQ** pulses high when a new sample is requested. **REQ** will pulse low when REQ_POL is high.
3	R/W	REQ_WIDTH	Normally the **REQ** pin will pulse high for two clock cycles. This control bit forces **REQ** to be high for "N/2" clocks. NOTE: the period of the **REQ** signal is either 4N or 2N clocks, depending upon whether the REAL_INPUT control bit is low or high in the input mode control register (See Section 5.5).
4	R/W	DIAG	Use the diagnostic ramp as the input source for the four channels. The ramp starts at -32768 and counts up to +32768 and starts over again. The ramp increments once every complex input cycle (every 4N clocks).
5	R/W	SO_OVF_MODE	When set, the SO bit will go low whenever an overflow occurs in the chip. Bits 6 & 7 of control register 32 of page 1 must be low to use this mode (see Section 5.14).
6,7	R/W	DIAG_SYNC	The diagnostic ramp is synchronized by the sync selected by these bits according to Table 1. This sync also loads the checksum register.

5.3 INTERPOLATION GAIN REGISTER

Register 2 controls the interpolation gain for the chip. These settings are common to all channels

ADDRESS 2: **Interpolation Gain**, *suggested default = 0x46*

BIT	TYPE	NAME	DESCRIPTION
0-3	R/W	SCALE	SCALE ranges from 0 to 15.
4,5	R/W	BIG_SHIFT	BIG_SHIFT equals 0, 1 or 2.
6	R/W	AUTO_FLUSH	The chip will automatically flush a channel if instability in the channel's CIC filter is detected and this bit is set.
7	R/W	MSB_INVERT	Inverts the MSB of the output data (OUT15) for use with offset binary DACs.

The CIC filter has a gain which is equal to N^3. To remove this gain the CIC outputs are shifted down by (3+SCALE+12*BIG_SHIFT) bits and then rounded to 16 bits before they are sent to the mixer circuit. The value chosen for BIG_SHIFT must also satisfy: $2^{(12*BIG\_SHIFT+18)} \geq N^3$. Overflows due to improper gain settings will go undetected if this relationship is violated. This restriction means that BIG_SHIFT = 0 for N between 8 and 64, BIG_SHIFT = 1 for N between 65 and 1024, and BIG_SHIFT = 2 for N between 1025 and 16384.

5.4 INTERPOLATION REGISTERS

Registers 3, and 4 contain the 14 bit interpolation ratio control.

ADDRESS 3: Interpolation Byte 0, *suggested default = 0x07*

BIT	TYPE	NAME	DESCRIPTION
0-7	R/W	**INT**[0:7]	The LSBs of the interpolation control

ADDRESS 4: Interpolation Byte 1, *suggested default = 0x00*

BIT	TYPE	NAME	DESCRIPTION
0-5	R/W	**INT**[8:13]	The 6 MSBs of the interpolation control
6,7	R	zero	Reads back zeros.

Where **INT** is equal to **N**-1. The chip interpolates the input data by a factor of 2N for real input data and 4N for complex input data, where N ranges from 8 to 16384. This provides an interpolation range from 32 to 65,536 for complex input signals and 16 to 32,768 for real input signals. **NOTE: The chip needs to be flushed each time the interpolation registers are changed.** See Section 5.8.

5.5 INPUT MODE REGISTER

This register controls the input bit serial format.

ADDRESS 5: Input Mode Register, *suggested default = 0x00*

BIT	TYPE	NAME	DESCRIPTION
0 LSB	R/W	PACKED	Puts the serial inputs into the 32 bit transfer mode where each complex pair is packed into 32 bit words. The complex pair is formatted as I word in the upper 16 bits and the Q word in the lower 16 bits. Each word is formatted as MSB first.
1	R/W	REAL_INPUT	The serial input accepts real data samples (not complex) when this bit is set. In this mode a single 16 bit word is expected after every **REQ** strobe, not a complex pair. The user has the option to enter real input samples as complex pairs and to not use the real input mode. If the complex mode (REAL_INPUT = 0) is used to enter real words, then the real samples should be alternately placed in the I and Q halves of the complex input pairs. NOTE: the REAL control bit in the interpolation mode register still needs set to enable real data up conversion.
2	R/W	SCK_POL	The **SIN** Input bits and **SFS** frame strobes are clocked in on the trailing edge of SCK when this bit is set. The rising edge is used when this bit is low.
3	R/W	SFS_POL	The **SFS** signal is treated as active low when this bit is set. Otherwise the signal is treated as active high.
4	R/W	PARALLEL_A	The parallel/Serial control for channel A.
5	R/W	PARALLEL_B	The parallel/Serial control for channel B.
6	R/W	PARALLEL_C	The parallel/Serial control for channel C.
7	R/W	PARALLEL_D	The parallel/Serial control for channel D.

The parallel/serial control is low for serial input and high for parallel input. See Section 5.12.

5.6 COUNTER MODE REGISTER

Registers 6, and 7 set the counter's cycle period.

ADDRESS 6: **Counter Byte 0***, suggested default = 0xff*

BIT	TYPE	NAME	DESCRIPTION
0-7	R/W	**CNT**[0:7]	The LSBs of the counter cycle period

ADDRESS 7: **Counter Byte 1***, suggested default = 0xff*

BIT	TYPE	NAME	DESCRIPTION
0-7	R/W	**CNT**[8:15]	The 8 MSBs of the counter cycle period

The chip's internal sync counter counts in cycles of 128(**CNT**+1) clocks. A terminal count signal (TC) is output at the end of each cycle. The counter can be synchronized to an external sync as specified in the Sync mode Register (See Section 5.1). If **CNT** is set so that 128(**CNT**+1) is a multiple of twice the interpolation ratio (i.e., a multiple of 16N), then the terminal count of this counter can be output on the $\overline{\textbf{SO}}$ pin and used to periodically synchronize multiple GC4114 chips.

5.7 CHANNEL SYNC REGISTERS

Registers 8,9,10 and 11 control the synchronization modes of the four channels. The sync modes described here are unique to each of the channels. The modes use the same settings as shown in Table 1 (See Section 5.1).

ADDRESS 8: **Channel-A Sync Modes***, suggested default = 0x5f*
ADDRESS 9: **Channel-B Sync Modes**
ADDRESS 10: **Channel-C Sync Modes**
ADDRESS 11: **Channel-D Sync Modes**

BIT	TYPE	NAME	DESCRIPTION
0,1 LSB	R/W	FREQ_SYNC	The new frequency setting takes affect on this sync
2,3	R/W	PHASE_SYNC	The new phase offset takes affect on this sync
4,5	R/W	NCO_SYNC	The NCO is initialized to the phase setting by this sync
6,7 MSB	R/W	DITHER_SYNC	The dither circuit is initialized by this sync to zero.

The NCO_SYNC is usually set to be always off, unless the user wants to coherently control the phases of multiple channels. The FREQ_SYNC and PHASE_SYNC are typically set to be always on so that frequency and phase settings will take effect immediately as they are written into their control registers (See Section 5.0 addresses 32 to 63). Alternately, the FREQ_SYNC and PHASE_SYNC controls may be set to the $\overline{\text{SI}}$ or one shot modes to allow the frequency and phase to be changed smoothly, or coherently with another event. The DITHER_SYNC is used to turn on or off the dithering of the NCO phase. To turn off dithering set the DITHER_SYNC to be always on so that it remains initialized to zero. To turn dithering on set the sync to be always off. During diagnostics the NCO_SYNC and DITHER_SYNC should be set to "TC".

5.8 CHANNEL FLUSH CONTROL REGISTER

This register controls flushing the four channels. Each channel is flushed when the selected sync occurs The sync is selected according to Table 1 in Section 5.1.

ADDRESS 12: Channel Flush Register, *suggested default = 0x55*

BIT	TYPE	NAME	DESCRIPTION
0,1 LSB	R/W	FLUSH_A[0:1]	The flush sync for channel A.
2,3	R/W	FLUSH_B[0:1]	The flush sync for channel B.
4,5	R/W	FLUSH_C[0:1]	The flush sync for channel C.
6,7 MSB	R/W	FLUSH_D[0:1]	The flush sync for channel D.

Each channel needs to be flushed when the chip is being initialized or when the interpolation control is changed. The flush lasts for 8N clocks after the sync occurs. The channel flush syncs will normally be left in a “never” mode. If a channel is unused, then the user should leave the channel in the “always” flush mode which will clear the datapath, clear the channel’s output, and lower its power consumption. During diagnostics the channels will need to be flushed at the beginning of each sync cycle.

5.9 SUMMER MODE REGISTER

This register controls the output summer and round circuit.

ADDRESS 13: Summer Mode Register, *suggested default = 0x09*

BIT	TYPE	NAME	DESCRIPTION
0,1 LSB	R/W	SUM_SCALE	The sum of the four channels is shifted down by SUM_SCALE bits before being added to the sum-in signal.
2	R/W	SUM_DELAY	The sum of the four channels is delayed by seven clock cycles when this bit is high. This allows the outputs of two chips to be coherently summed.
3	R/W	SUM_CLR	Clears the IN[0:15] inputs to the summer.
4	R/W	RND8	Round the output to 8 bits.
5	R/W	RND10	Round the output to 10 bits.
6	R/W	RND12	Round the output to 12 bits.
7 MSB	R/W	RND14	Round the output to 14 bits.

Only one of the round control bits should be set. If none are set, then the output is rounded to 16 bits. The lower bits are rounded into the upper bits. Bits below the rounding point are cleared.

5.10 STATUS CONTROL REGISTER

This register contains miscellaneous control and status information.

ADDRESS 14: Status Control Register, *suggested default = 0x08*

BIT	TYPE	NAME	DESCRIPTION
0 LSB	R/W	INPUT_READY	The user sets this bit after loading the input registers. The chip clears this bit when the values have been read and it is time to load new ones.
1	R/W	MISSED	The chip sets this bit If the user has not set the INPUT_READY bit before the chip reads the input registers. This bit high indicates that an error has occurred.
2	R/W	PD_CLOCK_OFF	Power_Down modes 0 and 1 normally use a 1 kHz keep alive clock. This clock is disabled when this bit is high.
3	R/W	EN_DOUBLER	Enables the clock doubling circuit. This bit defaults to low. The user must set the bit to enable the clock doubler.
4,5	R/W	PAGE	Selects the page mode for control addresses 32 to 63 as follows: **PAGE** — **MODE** 0 — Frequency, Phase and Gain 1 — Status and Test monitors 2 — Filter coefficients 0 to 15 3 — Filter coefficients 16 to 31
6,7	R/W	POWER_DOWN	This two bit field controls the power down and keep alive circuit as follows: POWER_DOWN — MODE 0 — Clock loss detect mode 1 — Power down mode 2 — Disabled 3 — Test The power_down bits default to 0 (clock loss detect mode) upon power up.

The INPUT_READY bit is used to tell an external processor when to load new input samples. If desired, the **REQ** pin can be used as an interrupt to the external processor (See Section 5.2) to tell the processor when to load new samples. The user does not need to set the INPUT_READY bit if **REQ** is used. If INPUT_READY is not set, however, the MISSED flag will not be valid. NOTE: the parallel input mode assumes the data is being entered as complex pairs, even when the data is real. To enter real data in the parallel mode, the user must put the real data into complex pairs, the first sample of each pair in the I-half and the second in the Q-half.

5.11 CHECKSUM REGISTER

The checksum register is a read only register which contains the checksum of the OUT[0:15] data. The checksum is stored in the checksum register and then starts over again each time the DIAG_SYNC (See Section 5.2) occurs. This is a read only register. For example diagnostic configurations see Section 7.6.

ADDRESS 15: Checksum Register

BIT	TYPE	NAME	DESCRIPTION
0-7	R	**CHECKSUM**[0:7]	The checksum.

5.12 CHANNEL INPUT REGISTERS

Addresses 16 through 31 are used to input values into the chip when the channels are in the parallel input mode. The inputs are 16 bit two's complement numbers which are loaded as two 8 bit bytes. The address assignments are:

ADDRESSES	NAME	ADDRESSES	NAME
16,17	Channel A, I-input	24,25	Channel C, I-input
18,19	Channel A, Q-input	26,27	Channel C, Q-input
20,21	Channel B, I-input	28,29	Channel D, I-input
22,23	Channel B, Q-input	30,31	Channel D, Q-input

These are all read/write registers.

5.13 PAGE ZERO (CHANNEL CONTROL) REGISTERS

Addresses 32 to 63 are used to load each channel's frequency, phase and gain settings when PAGE = 0 in the status register (see Section 5.10). The address assignments are:

ADDRESSES	NAME	ADDRESSES	NAME
32,33,34,35	FREQ_A[31:0]	48,49,50,51	FREQ_C[31:0]
36,37	PHASE_A[15:0]	52,53	PHASE_C[15:0]
38	GAIN_A[7:0]	54	GAIN_C[7:0]
39	unused	55	unused
40,41,42,43	FREQ_B[31:0]	56,57,58,59	FREQ_D[31:0]
44,45	PHASE_B[15:0]	60,61	PHASE_D[15:0]
46	GAIN_B[7:0]	62	GAIN_D[7:0]
47	unused	63	unused

The 32 bit frequency control words (FREQ_A, FREQ_B, FREQ_C and FREQ_D) are defined as:

$$FREQ = 2^{32}F/F_{CK}$$

where F is the desired center frequency of the channel and F_{CK} is the chip's clock rate (not the CK2X rate). Use negative frequency vales to invert the signal's spectrum. The 32 bit frequency words are entered as four bytes, the least significant byte in the lowest address, the most significant in the higher address.

The 16 bit phase offsets are defined as:

$$PHASE = 2^{16}P/2\pi$$

where P is the desired phase in radian from 0 to 2π.

The 8 bit gain is defined as:

$$GAIN = G/128$$

where G ranges from -128 to +127. Note that GAIN is only part of the chip's gain and should be used in conjunction with SCALE, BIG_SCALE, COARSE and SUM_SCALE. See Section 3.7 for details.

The channel control registers are read/write.

5.14 PAGE ONE (STATUS AND TEST) REGISTERS

Addresses 32 to 63 are used for status and test monitors when PAGE is set to one.

ADDRESS 32: Overflow Status, *suggested default = 0x00*

BIT	TYPE	NAME	DESCRIPTION
0	R/W	OVER_A	The chip sets this bit when an overflow occurs in channel A.
1	R/W	OVER_B	The chip sets this bit when an overflow occurs in channel B
2	R/W	OVER_C	The chip sets this bit when an overflow occurs in channel C
3	R/W	OVER_D	The chip sets this bit when an overflow occurs in channel D
4	R/W	OVER_SUM	The chip sets this bit when there is an overflow due to the SUM_SCALE setting being too low (See Section 5.9)
5	R/W	OVER_ROUND	The chip sets this bit if rounding the output causes an overflow.
6-7	R/W	-	Reserved for factory test. These bits must be zero to use SO_OVF_MODE (see Section 5.2)

The channel overflow is detected in the SCALE AND ROUND circuit of each CIC filter (See Section 3.4.3). The overflow bits must be cleared by the user before a new overflow will be detected.

ADDRESS 33: Clock Status

BIT	TYPE	NAME	DESCRIPTION
0	R	KACK	This bit monitors the keepalive clock.
1	R	KA_MODE	This bit monitors the keepalive mode. The chip sets this bit low when the keep alive circuit is activated.
2-7	-	unused	

ADDRESS 34: Mask Revision

BIT	TYPE	NAME	DESCRIPTION
0-7	R	REVISION	Mask revision number.

This address can be used to determine the mask revision number for the GC4114. The mask revision numbers are shown in Table 2 below (the mask codes are printed on the GC4114 package).

Table 2: Mask Revisions

Mask Revision Number (Address 34)	Release Date	Mask Code on Package	Description
0	July 1997	55531B	Original
0	March 1998	55531C	Metal 1 mask changed, no functional changes

ADDRESS 39,47,55,63: Test Points A, B, C and D

These test points are for factory tests to monitor the CIC filters. Not used for normal operation.

5.15 PAGES TWO AND THREE (COEFFICIENT) REGISTERS

The 32 user programmable filter coefficients are stored in addresses 32 to 63 when PAGE is set to 2 and 3. Page two is for coefficients 0 through 15 and page three is for coefficients 16 through 31, where coefficient 0 is the first coefficient and coefficient 31 is the middle coefficient of the filter's impulse response. The 16 bit coefficients are stored in two bytes, least significant byte first. For example, the LSBs of coefficient 0 are stored in address 32 and the MSBs in address 33. TO LOAD A COEFFICIENT THE USER MUST WRITE THE LSBYTE FIRST FOLLOWED BY THE MSBYTE. Unknown values will be written into the LSBs if the MSB is written first.

The coefficient registers are write only.

The coefficients should be entered after the chip has been configured by setting control registers 0 through 14 to their desired values. The coefficients should be written to the chip while FILTER_SELECT is cleared (bit 1 of address 1 described in Section 5.2 is set to 0). FILTER_SELECT is set to one after the coefficients have been loaded. Note that FILTER_SELECT must be low for at least 4N clock cycles whenever it is set low.

6.0 SPECIFICATIONS

6.1 ABSOLUTE MAXIMUM RATINGS

Table 3: Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
DC Supply Voltage	V_{CC}	-0.3	4.1	V	
Control I/O, CKMODE, SFS, SCK and SIN Supply Voltage	V_{UP}	-0.3	6.0	V	
Input voltage (undershoot and overshoot)	V_{IN}	-0.5	V_{CC}+0.5	V	1
Storage Temperature	T_{STG}	-65	150	°C	
Lead Soldering Temperature (10 seconds)			300	°C	

Notes:
1. MAX is V_{UP}+0.5 for the Control I/O, CKMODE and serial input pins.

6.2 RECOMMENDED OPERATING CONDITIONS

Table 4: Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
DC Supply Voltage	V_{CC}	3.1	3.5	V	1
Control I/O, CKMODE, SFS, SCK and SIN Supply Voltage	V_{UP}	V_{CC}	5.5	V	
Temperature Ambient, no air flow	T_A	-40	+85	°C	2
Junction Temperature	T_J		125	°C	2

1. DC and AC specifications are tested for this range. The GC4114 will operate at derated specifications for lower supply voltages.
2. Thermal management may be required for full rate operation, See Table 5 below

6.3 THERMAL CHARACTERISTICS

Table 5: Thermal Data

THERMAL CONDUCTIVITY	SYMBOL	GC4114-CQ		GC4114-PQ		UNITS
		0.5 Watt	1 Watt	0.5 Watt	1 Watt	
Theta Junction to Ambient	θja	54	40	40	32	°C/W
Theta Junction to Case	θjc	17	15	13	11	°C/W

Note: Air flow will reduce θ**ja** and is highly recommended.

6.4 DC CHARACTERISTICS

All parameters are industrial temperature range of -40 to 85 ^{O}C ambient unless noted.:

Table 6: DC Operating Conditions

PARAMETER	SYMBOL	Vcc = 3.3V		UNITS	NOTES
		MIN	MAX		
Voltage input low	V_{IL}		0.8	V	2
Voltage input high	V_{IH}	2.0		V	2,3
Input current (V_{IN} = 0V)	I_{IN}	Typical +/- 50		uA	2
Voltage output low (I_{OL} = 2mA)	V_{OL}		0.5	V	2
Voltage output high (I_{OH} = -2mA)	V_{OH}	2.4	3.3	V	2,4
Data input capacitance (All inputs except **CK**)	C_{IN}	Typical 4		pF	1
Clock input capacitance (**CK** input)	C_{CK}	Typical 10		pF	1

Notes:

1. Controlled by design and process and not directly tested. Verified on initial parts evaluation.
2. Each part is tested at 85^{O}C for the given specification.
3. For V_{UP}=5V, V_{IH}=2.5V for the Control I/O, CKMODE and ACK pins.
4. For V_{UP}=5V, V_{OH}=2.8V (MIN) and V_{OH}=5V (MAX) for the Control I/O and RDY pins.

6.5 AC CHARACTERISTICS

Table 7: AC Characteristics (-40 TO +85°C Ambient, unless noted)

PARAMETER	SYMBOL	3.1V to 3.5V		UNITS	NOTES
		MIN	MAX		
Clock Frequency	F_{CK}	Note 5	70	MHz	2, 3
Clock low period (Below V_{IL})	t_{CKL}	6		ns	1
Clock high period (Above V_{IH})	t_{CKH}	6		ns	1
Clock rise and fall times (V_{IL} to V_{IH})	t_{RF}		2	ns	1
Input setup before **CK** goes high (**IN** or **$\overline{SI}$**)	t_{SU}	2		ns	2
Input hold time after **CK** goes high	t_{HD}	1		ns	2
Serial Clock Frequency	F_{SCK}	0	75	MHz	2,9
Serial Clock low or high period	$t_{SCKL/H}$	5		ns	2,9
Serial Data Setup before SCK	t_{SSU}	2		ns	2,9
Serial Data Hold from SCK	t_{SHD}	2			2,9
Data output delay from rising edge of **CK**. (**OUT** or **$\overline{SO}$**)	t_{DLY}	2 Note 1	11 Note 2	ns	4
Control Setup before both **$\overline{CE}$**, **$\overline{WR}$** or **$\overline{RD}$** go low	t_{CSU}	3		ns	2, 8, 10
Control hold after **$\overline{CE}$**, **$\overline{WR}$** or **$\overline{RD}$** go high	t_{CHD}	3		ns	2, 8, 10
Control strobe (**$\overline{CE}$** or **$\overline{WR}$**) pulse width (Write operation)	t_{CSPW}	30		ns	2, 8, 10
Control output delay **$\overline{CE}$** and **$\overline{RD}$** low to **C** (Read Operation)	t_{CDLY}		45	ns	2, 6, 8, 10
Control tristate delay after **$\overline{CE}$** and **$\overline{RD}$** go high	t_{CZ}		10	ns	1
Quiescent supply current (V_{IN}=0 or V_{CC}, F_{CK} = 1KHz or POWER_DOWN=1)	I_{CCQ}		4	mA	1
Supply current (F_{CK} =50MHz, N=8)	I_{CC}		350	mA	2, 7

Notes:

1. Controlled by design and process and not directly tested. Verified on initial part evaluation.
2. Each part is tested at 85 degrees C for the given specification.
3. The chip may not operate properly at clock frequencies below MIN and above MAX.
4. Output load is 2mA. Delays are measured from the rising edge of the clock to the output level rising above or Falling below $V_{CC}/2$.
5. The minimum clock rate must satisfy $F_{CK}/(4N) > 1KHz$, where N is the CIC interpolation ratio.
6. Output load is 2mA.
7. Current changes linearly with voltage and clock speed: Icc (MAX) $= \left(\frac{VCC}{3.3}\right)\left(\frac{F_{CK}}{50M}\right)\left(1+\frac{78}{N+18}\right)\left(\frac{12+A}{16}\right)88mA$

   where A is the number of active channels (0 to 4) and N is the CIC interpolation ratio.
8. See timing diagram in Figure 2 and description in Section 3.1.
9. See timing diagram in Figure 3 and description in Section 3.2
10. Not tested for V_{UP} at 5 volts.

7.0 APPLICATION NOTES

7.1 POWER AND GROUND CONNECTIONS

The GC4114 chip is a very high performance chip which requires solid power and ground connections to avoid noise on the V_{CC} and GND pins. If possible the GC4114 chip should be mounted on a circuit board with dedicated power and ground planes and with at least two decoupling capacitors (0.01 and 0.1 μf) adjacent to each GC4114 chip. If dedicated power and ground planes are not possible, then the user should place decoupling capacitors adjacent to each V_{CC} and GND pair.

IMPORTANT

The GC4114 chip may not operate properly if these power and ground guidelines are violated.

7.2 STATIC SENSITIVE DEVICE

The GC4114 chip is fabricated in a high performance CMOS process which is sensitive to the high voltage transients caused by static electricity. These parts can be permanently damaged by static electricity and should only be handled in static free environments.

7.3 SYNCHRONIZING MULTIPLE GC4114 CHIPS

A system containing two or more GC4114 chips will need to be synchronized if coherent operation is desired. To synchronize multiple GC4114 chips connect all of the sync input pins together so they can be driven by a common sync strobe. The common sync strobe can be from an external source, or can be the sync output from one of the chips. If the sync output from one of the chips is used, then the user can choose to output a one shot sync pulse from that chip, or the terminal count from the chip's sync counter. If the terminal count is used, then the sync cycle must be a multiple of 8N and the FLUSH (Address 12), NCO_SYNC and DITHER_SYNC (Addresses 8, 9, 10 and 11) sync control bits must be set to "never" (see Table 1) after initial synchronization.

See Figure 10 in Section 7.5 for an example configuration of multiple chips and see Section 7.9 for a description of how to periodically synchronize multiple chips.

7.4 THERMAL MANAGEMENT

The junction temperature must be kept below 125 $^{\circ}$C for reliable operation. The chip's power dissipation should be calculated using the equation for supply current in Section 6.5 and then the chip's junction temperature can be calculated using the package's thermal conductivity shown in Section 6.3. At full rate operation (F_{CK}=70MHz) the power is 1.44 Watts and the junction to ambient rise is 32 degrees per Watt for the plastic package. This represents a rise of 46 degrees over ambient. This means that under these conditions the ambient temperature has to be less than 79 $^{\circ}$C. Air flow will decrease the thermal resistance by 10% to 40%, allowing ambient temperatures between 84°C and 97 $^{\circ}$C. Increasing the decimation ratio (N) or decreasing the number of active channels (A) will also allow a higher ambient temperature operation.

7.5 PULSE SHAPING AND MODULATING QPSK OR QAM DATA

The chip is designed to pulse shape and up-convert digital symbol data for BPSK, PSK, QPSK or QAM modulation types. The symbol data is entered into the chip as I/Q pairs either at the symbol rate (baud rate) in the 1X mode, or at twice the symbol rate in the 2X mode. The PFIR is used to pulse shape the data using a root-raised cosine (RRC) filter. A formula which calculates the RRC coefficients is:

$$\text{taps}(k) = \left[\frac{32767}{\pi(1-A)+4A}\right]\left[\frac{1}{(1-(4AR(31-k))^2)}\right]\left[\frac{\sin((31-k)R\pi(1-A))}{(31-k)R} + 4A\cos((31-k)R\pi(1+A))\right]$$

where A is the desired excess bandwidth (typically 0.35), R is the ratio of the sample rate out of the PFIR to the baud rate of the data (0.5 for the 1X mode and 0.25 for the 2X mode), and k is the tap number ranging from 0 to 62. Only taps 0 through 31 are needed by the chip. The tap weights for an excess bandwidth of 0.35 are given in Section 3.4.1.

The choice between entering the data at the baud rate (1X mode) or entering the data at twice the baud rate (2X mode), depends upon the amount of image rejection required by the application. If 70 dB image rejection is adequate (see Figure 9b in Section 3.5), then entering the data at the baud rate will work. If more image rejection is required, then the data should be entered at twice the baud rate by alternately entering symbol I/Q pairs and zeros. The 2X input mode has greater than 90 dB image rejection as shown in Figure 9c.

The sample rate out of the chip, which is the same as the clock rate of the chip (F_{CK}), is equal to 4BN in the 1X mode and 8BN in the 2X mode. The maximum baud rate accepted by the chip is, therefore, F_{CK}/4N in the 1X mode and is F_{CK}/8N in the 2X mode.

The following subsections give examples of how to configure and initialize the chip in both the 1X and 2X modes for an example QPSK signal with a baud rate of 25KHz and an output sample rate of 60MHz. These examples are for a configuration using four chips to modulate 16 channels of data. Figure 10 shows the suggested interconnection between the four chips.

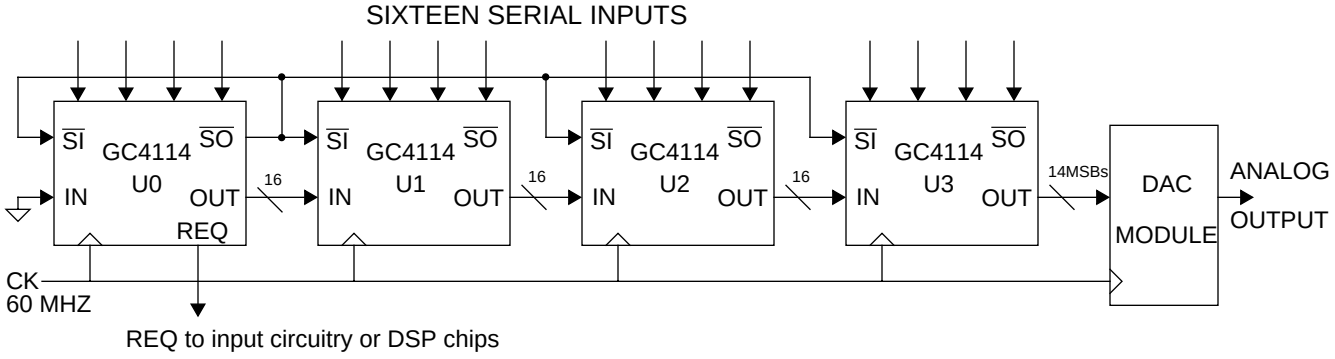


Figure 10. Sixteen Channel Modulator

Note that chip U0 provides the sync pulse that goes to all four chips. The REQ output from one of the chips (it will be the same from all four chips) must be used to synchronize the input serial data (see Section 3.2).

7.5.1 Modulating a 25K-Baud QPSK signal in the 1X Mode

This section illustrates how to modulate signals in the 1X mode. The signal parameters used in this example are shown in Table 8 below.

Table 8: Example QPSK Signal Parameters

Parameter	Symbol	Value	Units
Baud Rate	B	25	Kbaud
Excess Bandwidth	A	0.35	
Digital to Analog Converter (DAC) Size		14	Bits
Desired Crest Factor for the DAC	CF	0.2	(-14dB)
Number of Channels	M	16	

It is assumed that the QPSK symbols have been mapped into I/Q pairs as shown in Table 9. The value of

Table 9: QPSK Symbol Map

Symbol	I	Q
0	16384	16384
1	-16384	16384
2	16384	-16384
3	-16384	-16384

16384 is arbitrary, but should be greater than 8192 to allow reasonable gain settings.

The information in Tables 8 and 9 can be used to derive the CIC interpolation ratio (N) and the gain settings (G, SCALE, BIG_SHIFT and SUM_SCALE). The filter coefficients for the 1X mode root-raised cosine filter with an excess bandwidth of 0.35 can be derived using the formula shown above. These coefficients are listed in Section 3.4.1. The sum of these coefficients (PFIR_SUM) is used in the gain calculation and is equal to 59835.

In the 1X mode the clock rate is equal to 4BN, so N is 600 for F_{CK} equal to 60MHz and B equal to 25KHz. The optimal gain setting for the chip is described in Section 3.7. The first equation to be optimized is $CF = \left\{\frac{RMS}{32768}\right\}\left\{\frac{G}{128}\right\}\left\{\frac{PFIR\_SUM}{65536}\right\}$. The crest factor is 0.2, the RMS input level[1] is 16384, and the PFIR_SUM is 59835. Solving this equation for G gives a value of G=56. The second equation to satisfy is $CF = \left\{\frac{RMS}{32768}\right\}\left\{\frac{G}{128}\right\}\left\{\frac{PFIR\_SUM}{65536}\right\}\{N^3 2^{-(SCALE + 12 \times BIG\_SHIFT + 3)}\}$. The term N^3 is slightly less than 2^{28}, so a value of BIG_SHIFT=1 and SCALE=13 is appropriate. Solving this equation using the complex data's RMS level of 23170 gives G=49.

The sum tree gain (SUM_SCALE) should be set to keep the final RMS output level, after adding M signals together, at the desired crest factor. The RMS output level increases by $\sqrt{M}$, which for M=16 is a gain of 4. Setting SUM_SCALE=2 will cancel the gain of 4 in the sum tree and leave the crest factor at 0.25 (-12dB).

The suggested control register settings for the chip with these parameters are shown in Table 10.

1. The RMS level of the I data is 16384, the RMS level of the Q data is 16384, but the RMS level of the combined complex data is $\sqrt{2}$ times16384 = 23170. The RMS level of the combined data must be considered in the second equation in order to prevent overflow in the mixer.

Table 10: 1X QPSK Configuration

Control Registers		Channel, Status and Coefficient Pages				
Address	Data	Address	Page 0	Page 1	Page 2	Page 3
00 (HEX)	65 (HEX)[1]	20 (HEX)	A FREQ[0:7]	00	1B	8B
01	00->02[2]	21	A FREQ[8:15]	read only	00	FF
02	5D	22	A FREQ[16:23]		EC	08
03	57	23	A FREQ[24:31]		FF	00
04	02	24	00		FA	70
05	01[5]	25	00		FF	00
06	57	26	31		22	51
07	02	27			00	FF
08	5F	28	B FREQ[0:7]		E2	52
09	5F	29	B FREQ[8:15]		FF	00
0A	5F	2A	B FREQ[16:23]		F7	E0
0B	5F	1B	B FREQ[24:31]		FF	00
0C	55	2C	00		27	A4
0D	0A, 02, 82[3]	2D	00		00	FE
0E	P8[4]	2E	31		DB	3D
0F	read only	2F			FF	00
10	00	30	C FREQ[0:7]		FF	1E
11	00	31	C FREQ[8:15]		FF	01
12	00	32	C FREQ[16:23]		34	07
13	00	33	C FREQ[24:31]		00	FD
14	00	34	00		C9	FE
15	00	35	00		FF	02
16	00	36	31		FB	AC
17	00	37			FF	06
18	00	38	D FREQ[0:7]		3E	36
19	00	39	D FREQ[8:15]		00	F0
1A	00	3A	D FREQ[16:23]		B8	1B
1B	00	3B	D FREQ[24:31]		FF	F6
1C	00	3C	00		0F	01
1D	00	3D	00		00	47
1E	00	3E	31		5C	FF
1F	00	3F			00	7F

1. Initialize to 65 in chip U0 (Master) while configuring the chips, then set to E5 to fire off the one shot pulse, then back to 65.This assumes that $\overline{SO}$ is tied to $\overline{SI}$ of all four chips
2. Initialize to 00, then set to 02 after generating the one shot pulse.
3 Chip U0 uses 0A for SUM_CLR, U1 and U2 use 02 for sum I/O mode, and U3 uses 82 for round to 14 bits.
4. “P” is the page number. The lower nibble should stay at “8¨.
5. Serial interface dependent.

The initialization procedure is to load all control and coefficient registers in all four chips as shown in Table 10, and then to synchronize all of the chips using the one shot pulse from chip U0, and then to go back and write 02_{HEX} into address 1 of each chip to select the downloaded coefficients. The one shot pulse is generated by setting address 0 in chip U0 to $E5_{HEX}$ and then back to 65_{HEX}.

7.5.2 Modulating a 25K-Baud QPSK signal in the 2X Mode

This section illustrates how to modulate signals in the 2X mode. The signal parameters are the same as shown in Tables 8 and 9 except that the data is entered into the chip at twice the baud rate (50 KHz) by alternating

between symbol data and zeros. This cuts the interpolation ratio in half, so that the CIC interpolation ratio N is 300 instead of 600. The root-raised-cosine filter coefficients can be derived using the formula in Section 7.5 with R set to 0.25. These coefficients are listed in Section 3.4.1. The PFIR_SUM value for this set of coefficients is 119387

The alternating with zeroes causes the RMS amplitude of the inputs to decrease by a factor of two. Evaluating the first gain equation in Section 7.5.2 using the new RMS and PFIR_SUM values gives G = 56. In the second equation the term N^3 is slightly less than 2^{25}, so BIG_SHIFT=1 and SCALE=10 is appropriate. Solving for G gives G = 49. The suggested control register settings for the chip with these parameters are shown in Table 11.

Table 11: 2X QPSK Configuration

Control Registers		Channel, Status and Coefficient Pages				
Address	Data	Address	Page 0	Page 1	Page 2	Page 3
00 (HEX)	65 (HEX)[1]	20 (HEX)	A FREQ[0:7]	00	F4	8E
01	00->02[2]	21	A FREQ[8:15]	read only	FF	01
02	5A	22	A FREQ[16:23]		8B	1E
03	2B	23	A FREQ[24:31]		FF	01
04	01	24	00		8F	E2
05	01[5]	25	00		FF	FE
06	2B	26	31		08	07
07	01	27			00	FD
08	5F	28	B FREQ[0:7]		7F	46
09	5F	29	B FREQ[8:15]		00	FE
0A	5F	2A	B FREQ[16:23]		70	FE
0B	5F	1B	B FREQ[24:31]		00	02
0C	55	2C	00		DA	A2
0D	0A, 02, 82[3]	2D	00		FF	07
0E	P8[4]	2E	31		51	AC
0F	read only	2F			FF	06
10	00	30	C FREQ[0:7]		7A	6C
11	00	31	C FREQ[8:15]		FF	FD
12	00	32	C FREQ[16:23]		52	36
13	00	33	C FREQ[24:31]		00	F0
14	00	34	00		13	F7
15	00	35	00		01	E9
16	00	36	31		E0	1B
17	00	37			00	F6
18	00	38	D FREQ[0:7]		B9	2B
19	00	39	D FREQ[8:15]		FF	18
1A	00	3A	D FREQ[16:23]		A4	01
1B	00	3B	D FREQ[24:31]		FE	47
1C	00	3C	00		CD	D1
1D	00	3D	00		FE	6F
1E	00	3E	31		3D	FF
1F	00	3F			00	7F

1. Initialize to 65 in chip U0 (Master) while configuring the chips, then set to E5 to fire off the one shot pulse, then back to 65.This assumes that $\overline{SO}$ is tied to $\overline{SI}$ of all four chips
2. Initialize to 00, then set to 02 after generating the one shot pulse.
3. Chip U0 uses 0A for SUM_CLR, U1 and U2 use 02 for sum I/O mode, and U3 uses 82 for round to 14 bits.
4. “P” is the page number. The lower nibble should stay at “8¨.
5. Serial interface dependent.

7.6 DIAGNOSTICS

Four diagnostic tests are described here. These tests use the diagnostic ramp as the input data source and the counter for synchronization. The tests are run by loading the configurations, waiting for the checksum to stabilize (about 4 million clock cycles), and then reading the checksum from address 15 and comparing it to the expected checksum shown in each configuration table for address 15:

Table 12: Diagnostic Test 1 Configuration

Control Registers		Channel, Status and Coefficient Pages				
Address	Data	Address	Page 0	Page 1	Page 2	Page 3
00 (HEX)	2A (HEX)	20 (HEX)	55	00	unused	
01	90	21	AA	read only		
02	07	22	55			
03	07	23	AA			
04	00	24	55			
05	00	25	AA			
06	FF	26	55			
07	0F	27	00			
08	AA	28	AA			
09	AA	29	55			
0A	AA	2A	AA			
0B	AA	1B	55			
0C	AA	2C	AA			
0D	0A	2D	55			
0E	08	2E	AA			
0F	**15**[1]	2F	00			
10	00	30	55			
11	00	31	AA			
12	00	32	55			
13	00	33	AA			
14	00	34	55			
15	00	35	AA			
16	00	36	55			
17	00	37	00			
18	00	38	AA			
19	00	39	55			
1A	00	3A	AA			
1B	00	3B	55			
1C	00	3C	AA			
1D	00	3D	55			
1E	00	3E	AA			
1F	00	3F	00			

1. This is the read-only expected checksum.

:

Table 13: Diagnostic Test 2 Configuration

Control Registers		Channel, Status and Coefficient Pages				
Address	Data	Address	Page 0	Page 1	Page 2	Page 3
00 (HEX)	2A (HEX)	20 (HEX)	01	00	unused	
01	90	21	23	read only		
02	10	22	45			
03	0F	23	67			
04	00	24	89			
05	02	25	AB			
06	FF	26	CD			
07	0F	27	00			
08	AA	28	EF			
09	AA	29	01			
0A	AA	2A	23			
0B	AA	1B	45			
0C	AA	2C	67			
0D	08	2D	89			
0E	08	2E	AB			
0F	**46**[1]	2F	00			
10	00	30	CD			
11	00	31	EF			
12	00	32	01			
13	00	33	23			
14	00	34	45			
15	00	35	67			
16	00	36	89			
17	00	37	00			
18	00	38	AB			
19	00	39	CD			
1A	00	3A	EF			
1B	00	3B	01			
1C	00	3C	23			
1D	00	3D	45			
1E	00	3E	67			
1F	00	3F	00			

1. This is the read-only expected checksum.

:

Table 14: Diagnostic Test 3 Configuration

Control Registers		Channel, Status and Coefficient Pages				
Address	Data	Address	Page 0	Page 1	Page 2	Page 3
00 (HEX)	2A (HEX)	20 (HEX)	AA	00	55	AA
01	90->92[2]	21	55	read only	AA	55
02	11	22	AA		AA	55
03	1F	23	55		55	AA
04	00	24	AA		AA	55
05	00	25	55		55	AA
06	FF	26	AA		55	AA
07	0F	27	00		AA	55
08	AA	28	55		55	AA
09	AA	29	AA		AA	55
0A	AA	2A	55		AA	55
0B	AA	1B	AA		55	AA
0C	AA	2C	55		AA	55
0D	08	2D	AA		55	AA
0E	08	2E	55		55	AA
0F	**5A**[1]	2F	00		AA	55
10	00	30	AA		55	AA
11	00	31	55		AA	55
12	00	32	AA		AA	55
13	00	33	55		55	AA
14	00	34	AA		AA	55
15	00	35	55		55	AA
16	00	36	AA		55	AA
17	00	37	00		AA	55
18	00	38	55		55	AA
19	00	39	AA		AA	55
1A	00	3A	55		AA	55
1B	00	3B	AA		55	AA
1C	00	3C	55		AA	55
1D	00	3D	AA		55	AA
1E	00	3E	55		55	AA
1F	00	3F	00		AA	55

1. This is the read-only expected checksum.
2. Initialize to 90, load remaining registers and coefficients, wait 32 clock cycles, and then set to 92

:

Table 15: Diagnostic Test 4 Configuration

Control Registers		Channel, Status and Coefficient Pages				
Address	Data	Address	Page 0	Page 1	Page 2	Page 3
00 (HEX)	2A (HEX)	20 (HEX)	23	00	AA	55
01	90->92[2]	21	45	read only	55	AA
02	07	22	67		55	AA
03	07	23	89		AA	55
04	00	24	AB		55	AA
05	02	25	CD		AA	55
06	FF	26	37		AA	55
07	0F	27	00		55	AA
08	AA	28	01		AA	55
09	AA	29	23		55	AA
0A	AA	2A	45		55	AA
0B	AA	1B	67		AA	55
0C	AA	2C	89		55	AA
0D	08	2D	AB		AA	55
0E	08	2E	EF		AA	55
0F	**E5**[1]	2F	00		55	AA
10	00	30	EF		AA	55
11	00	31	01		55	AA
12	00	32	23		55	AA
13	00	33	45		AA	55
14	00	34	67		55	AA
15	00	35	89		AA	55
16	00	36	CD		AA	55
17	00	37	00		55	AA
18	00	38	CD		AA	55
19	00	39	EF		55	AA
1A	00	3A	01		55	AA
1B	00	3B	23		AA	55
1C	00	3C	45		55	AA
1D	00	3D	67		AA	55
1E	00	3E	AB		AA	55
1F	00	3F	00		55	AA

1. This is the read-only expected checksum.
2. Initialize to 90, load remaining registers and coefficients, wait 32 clock cycles, and then set to 92

7.7 OUTPUT TEST CONFIGURATION

The following configuration allows the user to debug the output interface to insure that the GC4114 data is being received properly by the following circuitry. The configuration in the following table will generate a fixed output sequence of sixteen values which will repeat indefinitely: *Note that all coefficients except the last two are zero*.

Table 16: Output Test Configuration

Control Registers		Channel, Status and Coefficient Pages				
Address	Data	Address	Page 0	Page 1	Page 2	Page 3
00 (HEX)	6A->EA->6A[1]	20 (HEX)	00	00	00	00
01	00->02[2]	21	00	read only	00	00
02	46	22	00		00	00
03	07	23	80		00	00
04	00	24	00		00	00
05	F0	25	00		00	00
06	FF	26	80		00	00
07	FF	27	00		00	00
08	EF	28	00		00	00
09	EF	29	00		00	00
0A	EF	2A	00		00	00
0B	EF	1B	00		00	00
0C	FE	2C	00		00	00
0D	08	2D	00		00	00
0E	08	2E	00		00	00
0F	read only	2F	00		00	00
10	AA	30	00		00	00
11	AA	31	00		00	00
12	00	32	00		00	00
13	00	33	00		00	00
14	00	34	00		00	00
15	00	35	00		00	00
16	00	36	00		00	00
17	00	37	00		00	00
18	00	38	00		00	00
19	00	39	00		00	00
1A	00	3A	00		00	00
1B	00	3B	00		00	00
1C	00	3C	00		00	00
1D	00	3D	00		00	C0
1E	00	3E	00		00	00
1F	00	3F	00		00	80

1. After configuring the chip fire off the one shot by setting to EA, then back to 6A.
2. Initialize to 00, send the one shot, wait at least 4N clocks, and then set to 02.

To run this test load all control registers and coefficient registers as shown above, then generate the one shot by setting address 0 to 0xEA and then back to 0x6A, and then enabling the programmable coefficients by setting address 1 to 0x02. After approximately 256 clock cycles the output will settle out and repeat the following 16 sample sequence (Note the alternating pattern in all bits except the 2 LSBs):

```
0x5556 0xaaaa 0x5556 0xaaaa 0x5556 0xaaaa 0x5556 0xaaaa
0x5556 0xaaa9 0x5557 0xaaa9 0x5557 0xaaa9 0x5557 0xaaa9
```

7.8 INPUT TEST CONFIGURATION

The serial input configuration and timing can be checked using the following configuration. The input data is the I/Q pair 0xAA00 and 0x5500. The following configuration will output a known constant if that complex pair is received correctly. For power of 2 interpolation ratios and where SCALE and BIG_SCALE are set to satisfy: $N^3 = 2^{(SCALE+BIG\_SHIFT*12+3)}$, the constant is 0x9090. For non power of 2 ratios or for other SCALE and BIG_SHIFT settings the constant can be determined as described below. *Note that all coefficients except the last two are zero.*

Table 17: Input Test Configuration

Control Registers		Channel, Status and Coefficient Pages				
Address	Data	Address	Page 0	Page 1	Page 2	Page 3
00 (HEX)	6A->EA->6A[1]	20 (HEX)	00	00	00	00
01	00->02[2]	21	00	read only	00	00
02	46	22	00		00	00
03	07	23	00		00	00
04	00	24	00		00	00
05	F0[3]	25	30		00	00
06	FF	26	80		00	00
07	FF	27	00		00	00
08	EF	28	00		00	00
09	EF	29	00		00	00
0A	EF	2A	00		00	00
0B	EF	1B	00		00	00
0C	FE	2C	00		00	00
0D	88	2D	00		00	00
0E	08	2E	00		00	00
0F	read only	2F	00		00	00
10	00	30	00		00	00
11	AA	31	00		00	00
12	00	32	00		00	00
13	55	33	00		00	00
14	00	34	00		00	00
15	00	35	00		00	00
16	00	36	00		00	00
17	00	37	00		00	00
18	00	38	00		00	00
19	00	39	00		00	00
1A	00	3A	00		00	00
1B	00	3B	00		00	00
1C	00	3C	00		00	00
1D	00	3D	00		00	C0
1E	00	3E	00		00	00
1F	00	3F	00		00	80

1. After configuring the chip fire off the one shot by setting to EA, then back to 6A.
2. Initialize to 00, send the one shot, wait at least 4N clocks, and then set to 02.
3. Use F0 to calibrate the expected output and then change to the desired serial input configuration.

To use this configuration change addresses 2, 3 and 4 to reflect the desired interpolation and gain values, but leave the serial controls set to 0xF0 in address 5. The value on the OUT pins should be a constant. Record that value and then configure address 5 to match the characteristics of desired the serial input format. If the serial

interface is working, then the output should be the same as was recorded. The expected value is 0x9090 for power of 2 interpolation ratios. For the QPSK 1X mode described in Section 7.5 with addresses 2, 3 and 4 set to 0x5A, 0x2B and 0x01 respectfully, the output should be 0xA654. The same value is expected for the 2X QPSK mode where addresses 2, 3, and 4 are 0x5D, 0x57 and 0x02 respectfully.

7.9 PERIODIC SYNC MODE

The configuration shown in Figure 10 allows all four chips to be synchronized to the master chip's $\overline{SO}$ output. This connection allows the system to be periodically synchronized by the master chip using its internal counter. By periodically synchronizing the system the user can insure that all of the chips will return to being in sync, even if one chip is thrown out of sync by noise, alpha particles or other factors such as lightning.

In the periodic sync mode the chips are configured so that the interpolation control counter (bits 0 and 1 of address 0) is synchronized by $\overline{SI}$, but all other syncs are set to ignore $\overline{SI}$ (set to "never" in Table 1). The internal counter registers (addresses 6 and 7) should be set to count in cycles equal to multiples of the interpolation factor **N**. The suggested counter setting is to set **CNT** equal to **INT** (See Sections 5.4 and 5.6). This will result in a periodic sync every 128**N** clocks (every 32 complex inputs). The sync output control (bits 4 and 5 of address 0) should be set to 2 (TC), and the USE_ONESHOT mode should be turned off. The FLUSH (address 12), NCO_SYNC and DITHER_SYNC (addresses 8, 9, 10, and 11) must be set to never.

The suggested initialization procedure for using the periodic sync mode is to configure the chips in the normal mode (see for example Tables 10 and 11), send the one shot pulse, wait 8 clock cycles for the chips to become synchronized, set up the periodic sync mode for all registers except address 0 (also set the FILTER_SELECT bit if necessary in address 1), and then put address 0 in the periodic sync mode. Table 18 shows the necessary settings.

Table 18: Periodic Sync Initialization Procedure

Control Address	Initial Normal Mode Settings in all Chips	Generate One Shot in Chip U0 only	Wait 8 clocks, Then Change Syncs in all chips to:	Then Change chip U0 To the Periodic Mode
00 (HEX)	65	E5	65	21
01	00[1]		02[2]	
02	46[3]			
03	INT			
04				
05	01[4]			
06	INT			
07				
08	5F		0F	
09	5F		0F	
0A	5F		0F	
0B	5F		0F	
0C	55		00	
0D	0A, 02, 42[3]			

1.Configure REQ_POL, REQ_WIDTH and REAL as necessary.
2. Set FILTER_SELECT as necessary.
3. Set to the appropriate SCALE, BIG_SCALE and AUTO_FLUSH values.
4. Set as necessary for the desired input format.
3. For example, chip U0 uses 0A for SUM_CLR, U1 and U2 use 02 for sum I/O mode, and U3 uses 42 for round to 12 bits.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
GC4114-PQ	OBSOLETE	LQFP	PZ	100		TBD	Call TI	Call TI

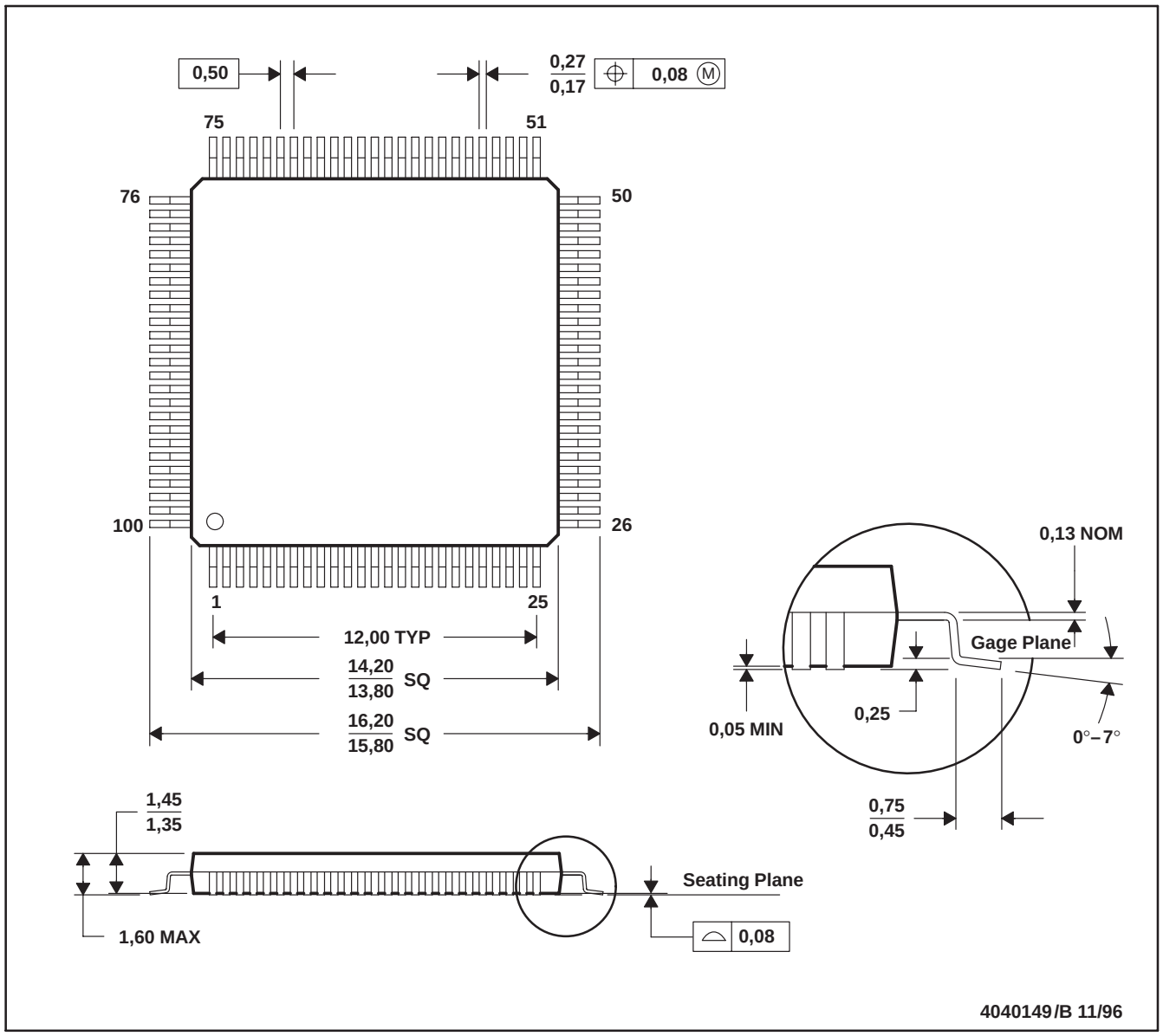
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

MTQF013A – OCTOBER 1994 – REVISED DECEMBER 1996

PZ (S-PQFP-G100) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

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